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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM, MLB, MBP15

04/24/2007

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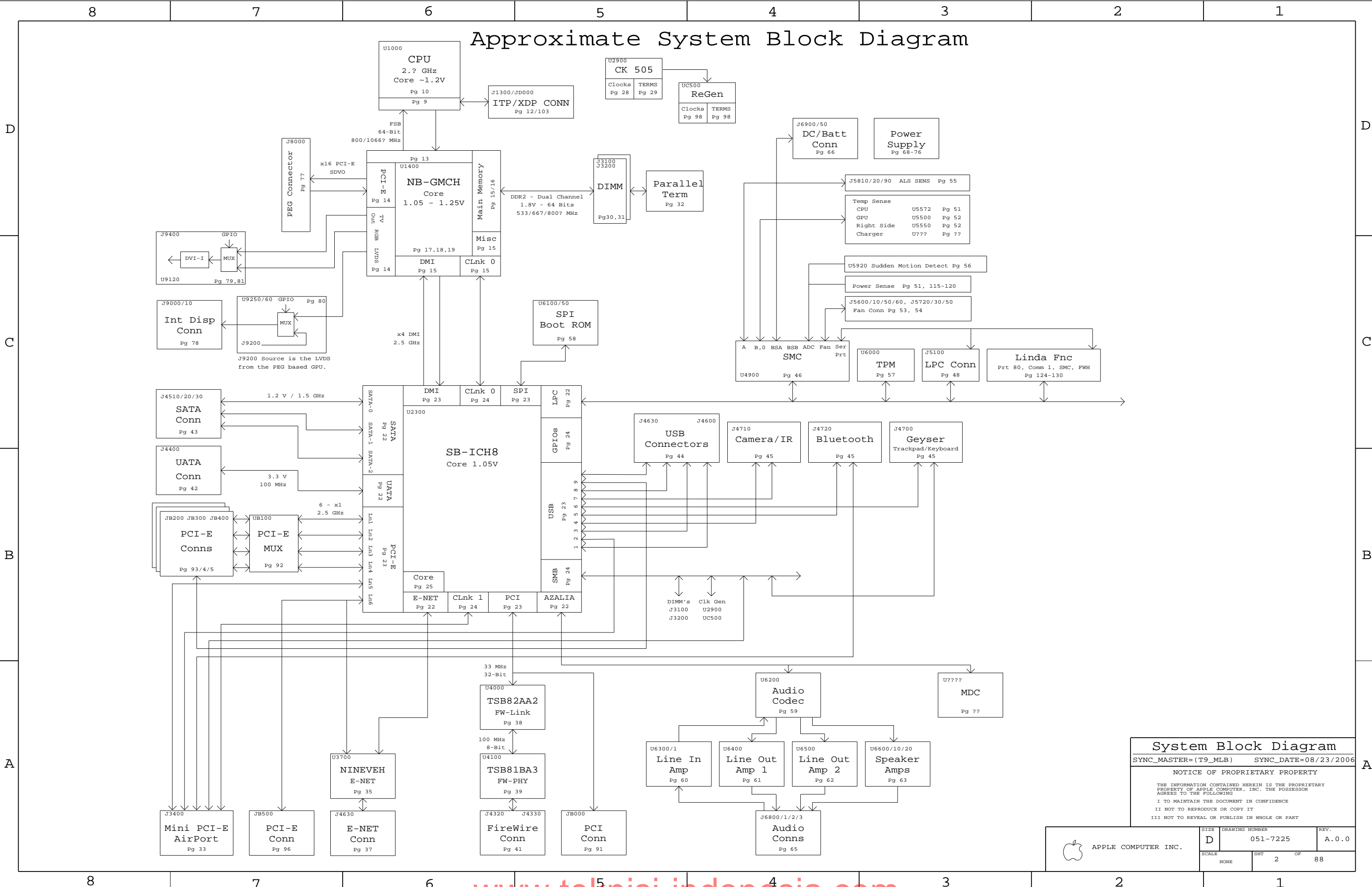
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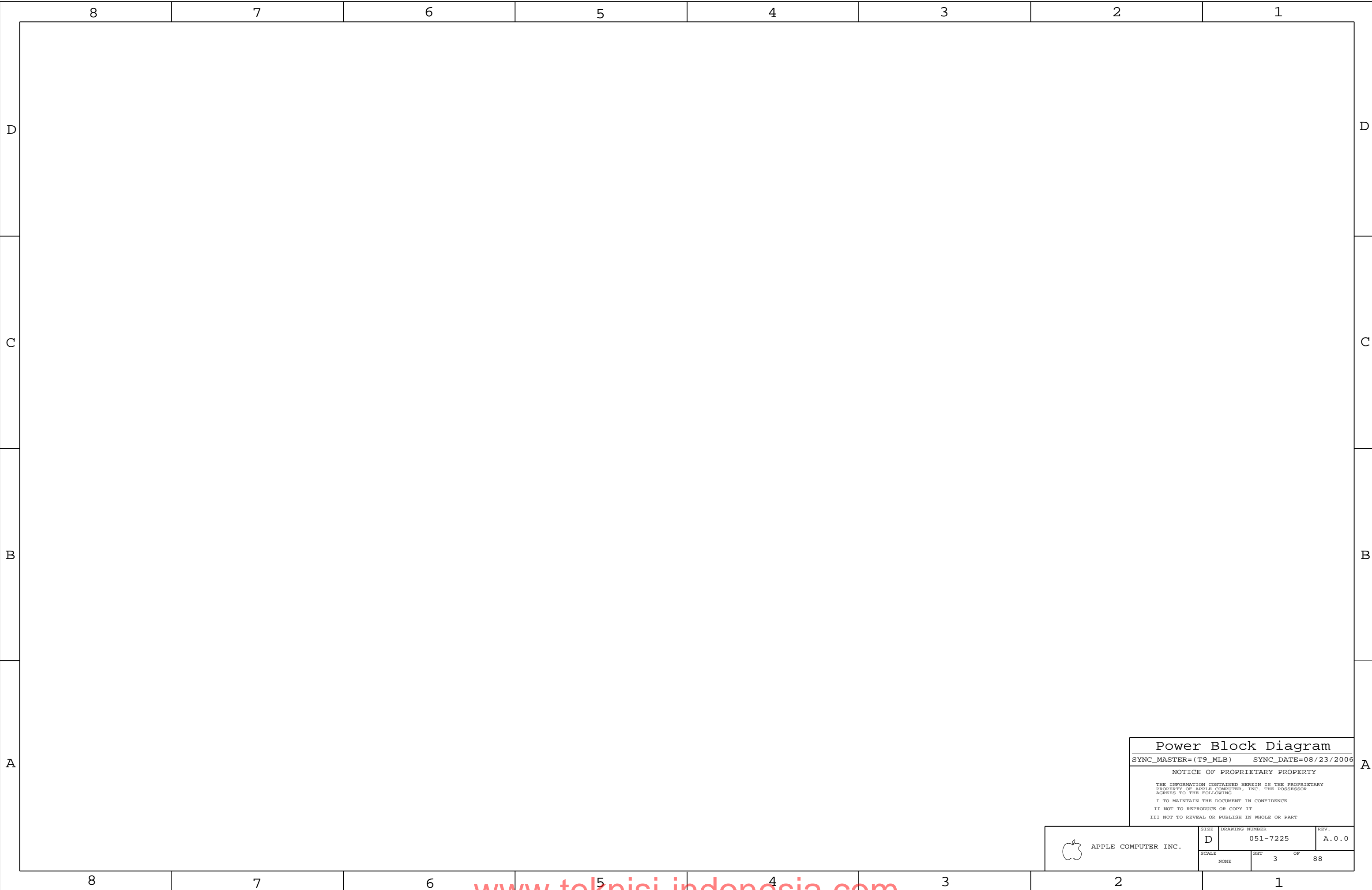
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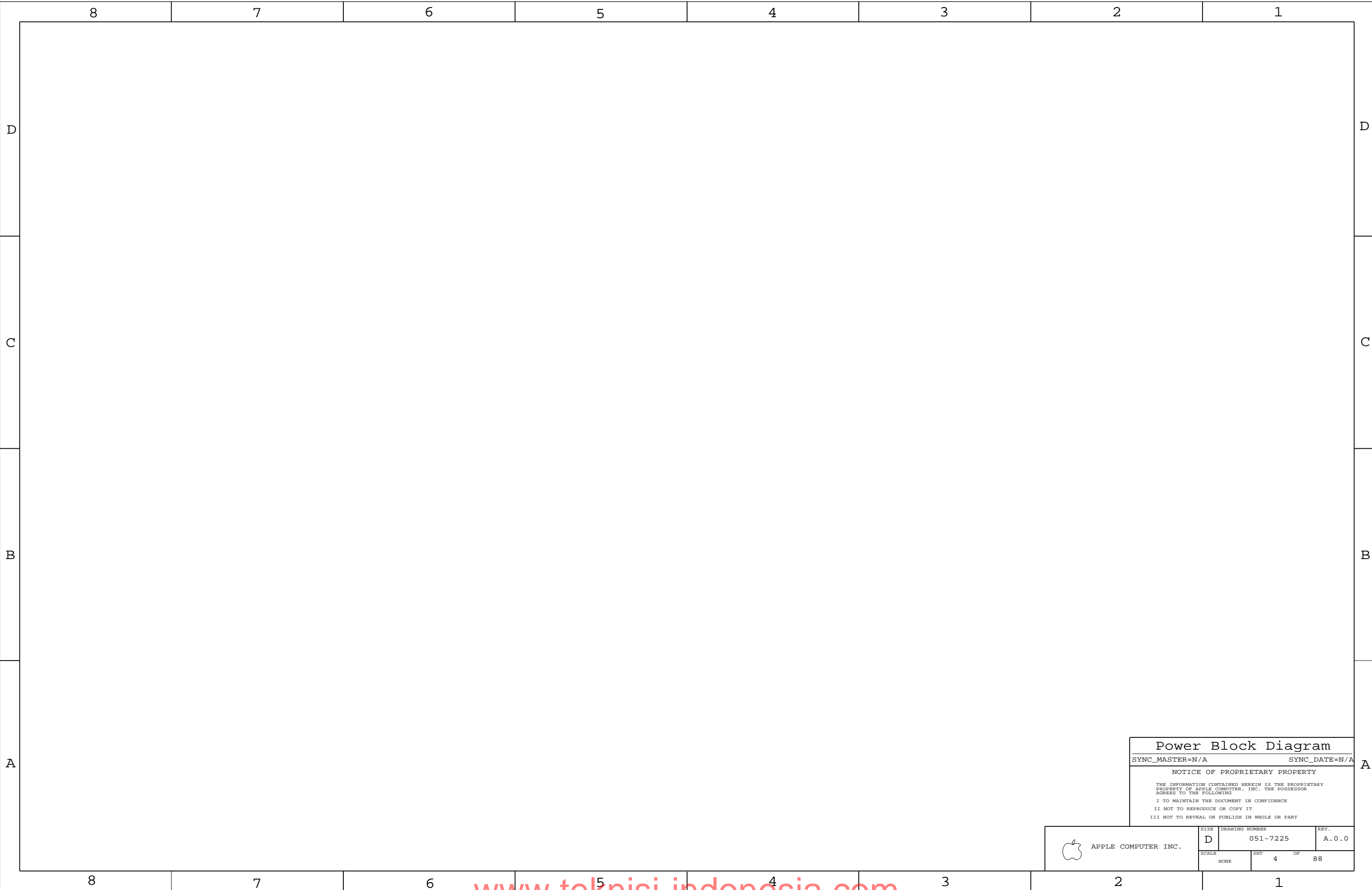
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7931	PCBA, 2.2GHZ, 128SAM_VRAM, M75, MBP15	M75_COMMON, EEE_X5D, CPU_2_2GHZ, FB_128_SAMSUNG
630-7932	PCBA, 2.4GHZ, 256SAM_VRAM, M75, MBP15	M75_COMMON, EEE_X5E, CPU_2_4GHZ, FB_256_SAMSUNG
630-8659	PCBA, 2.2GHZ, 128HY_VRAM, M75, MBP15	M75_COMMON, EEE_XXS, CPU_2_2GHZ, FB_128_HYNIX
630-8662	PCBA, 2.4GHZ, 256HY_VRAM, M75, MBP15	M75_COMMON, EEE_XXT, CPU_2_4GHZ, FB_256_HYNIX

M75 BOM Groups

BOM GROUP	BOM OPTIONS
M75_COMMON	ALTERNATE, COMMON, M75_COMMON1, M75_COMMON2, M75_DEBUG, M75_PROGPARTS
M75_COMMON1	EXTGPU_RST_HW, ISL9504B, LVDS_SEL_RESUME, ONEWIRE_PU
M75_COMMON2	P1V8S3_1V825, SLG2AP101, SMS_MOT_DIS, YUKON_ULTRA, VGA_TERM_CONN
M75_DEBUG	SMC_DEBUG_NO, XDP, LPCPLUS
M75_PROGPARTS	BOOTROM_PROG, SMC_PROG

BOM GROUP	BOM OPTIONS
FB_128_SAMSUNG	VRAM_128, VRAM_SAMSUNG, VRAM_128_SAMSUNG
FB_128_HYNIX	VRAM_128, VRAM_HYNIX, VRAM_128_HYNIX
FB_256_SAMSUNG	VRAM_256, VRAM_SAMSUNG, VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM_256, VRAM_HYNIX, VRAM_256_HYNIX

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:X5D]	CRITICAL	EEE_X5D
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:X5E]	CRITICAL	EEE_X5E
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:XXS]	CRITICAL	EEE_XXS
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:XXT]	CRITICAL	EEE_XXT

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3464	1	IC, MDC, SR, E1, PRQ, 2.2G, 35W, 800FSB, 4M, BGA	U1000	CRITICAL	CPU_2_2GHZ
337S3465	1	IC, MDC, SR, E1, PRQ, 2.4G, 35W, 800FSB, 4M, BGA	U1000	CRITICAL	CPU_2_4GHZ
338S0388	1	IC, GPU, NV G84M, BGA	U8000	CRITICAL	
338S0432	1	IC, NB, CRESTLINE, GM, CO, PRQ, 965PM	U1400	CRITICAL	
338S0434	1	IC, SB, ICH8M, B1, PRQ, BGA	U2300	CRITICAL	
353S1461	1	IC, ISL9504, SYNC REG CTRL, 2PHAS, QFN48, LF	U7100	CRITICAL	ISL9504A
353S1651	1	IC, ISL9504B, 2PH IMVP6 REG, PMON, QFN48	U7100	CRITICAL	ISL9504B
359S0127	1	IC, 68 PIN, CK505, LOW POWER CLOCK GENER	U2900	CRITICAL	SLG8LP537
359S0130	1	IC, SLG2AP101, LM PWR CLCK GEN, CK505, QFN68	U2900	CRITICAL	SLG2AP101
338S0386	1	IC, 88E8058, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	
338S0274	1	IC, SMC, HS8/2116	U4900	CRITICAL	SMC_BLANK
341S2004	1	IC, SMC, DEVELOPMENT, M75	U4900	CRITICAL	SMC_PROG
335S0384	1	IC, 16MBIT 8-PIN SPI SERIAL FLASH, SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2002	1	IC, EFI ROM, DEVELOPMENT, M75	U6100	CRITICAL	BOOTROM_PROG

333S0404	4	IC, SGRAM, GDDR3, 8Mx32, 700MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_128_SAMSUNG
333S0409	4	IC, SGRAM, GDDR3, 8Mx32, 700MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_128_HYNIX
333S0382	4	IC, SGRAM, GDDR3, 16Mx32, 700MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_SAMSUNG
333S0401	4	IC, SGRAM, GDDR3, 16Mx32, 700MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_HYNIX

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0011	157S0030		ALL	ESD alt to TOK/BI-Tech magnetec
152S0476	152S0276		ALL	Inductor alternate
353S1681	353S1294		ALL	TI alt to National
138S0603	138S0602		ALL	Murata alt to Samsung

BOM Configuration

SYNC_MASTER=N/A

SYNC_DATE=N/A

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PROTO

See Perforce change notes for updates before Proto Release
12/22/06 -- Released for Proto (Schem Rev 08, PCB Rev 01)

EVT

8.1.0:
01/05/07 -- Clock Termination: Removed NO STUFF property from R3067
01/05/07 -- GPU FB: Corrected FB CLK termination (added cap and removed connection to VDDQ)
8.2.0:
01/08/07 -- GPU FB: Added VREF support for unterminated memory mode (added FETs and pulldown Rs)
9.0.0:
01/09/07 -- Temp Sensors: NO STUFFed C5520 (circuit should have only 1 cap)
01/12/07 -- Power Aliases: Moved Ethernet to PP3V3_S3 from S5 (layout improvements)
01/12/07 -- Power Supplies: Minor power supply feedback connection changes from M76
9.1.0:
01/17/07 -- Power Aliases: Moved LCD panel FET to PP3V3_S5 from S0
01/17/07 -- SMBus: Changed R5260 & R5261 from 4.7K to 3.3K
01/17/07 -- Sync with T9 noME (6.1.4) to pull in WOL_EN and Wake-on-Wireless support
01/17/07 -- Power FETs: Corrected BOM values for 5V/3.3V S3/S0 FETs
01/17/07 -- Power Sequencing: Added RC delay on PP1V8_S3 switcher enable
01/17/07 -- Testpoints: Removed FUNC_TEST from NB_RESET_L and FSB_DPWR_L per PCB request
01/17/07 -- BOM: Consolidated 3 caps on page 59 from 132S0120 to 132S0131
01/17/07 -- BOM: Added Hynix BOM configurations
9.2.0:
01/17/07 -- Power Aliases: Deleted alias that accidentally eliminated filtering on PP1V5_S0_SB_VCC1_5_B
01/18/07 -- Clock Termination: Changed series termination on all single ended clocks to 33 ohms
01/18/07 -- IMVP: Updated BOMPTIONs and values for ISL9504B
01/18/07 -- Testpoints: Added NO_TEST property to LVDS_L_DATA_N<1>, _N<2>, _P<2> due to lack of layout space for TP
01/18/07 -- ODD Conn: Reconnected ODD power FET gate control circuitry to properly implement soft start (added one cap)
9.3.0:
01/19/07 -- SB Decoupling: Removed filtering for PP1V5_S0_SB_VCCGLANPLL to enable PP1V5_S0 corrections at SB
01/19/07 -- Ethernet Conn: Changed resistor short reference designators from R392x to RX392x
01/19/07 -- Clock Termination: Changed R3050 and R3055 to bypass discrete muxes for pending change to SLG2AP101
01/19/07 -- Power Sequencing: Added C7859 to create RC delay for 1.5 and 1.05V S0 rails
01/19/07 -- Power Sequencing: Changed power rail for U7850 to PP3V3_S5 to eliminate a leakage path
9.4.0:
01/19/07 -- GPU GPIOs: Added 2 TP's on GPIOs to make G-state externally visible
01/19/07 -- SB GPIOs: Changed SB_GPIO42 to WOW_EN and changed pullup to pulldown (T9_noME change 40787)
9.5.0:
01/22/07 -- LIO Conn: Removed unnecessary aliases as T9 reference design now matches M75 (T9_noME change 40998)
01/22/07 -- Clocks: Changed U2900 to SLG2AP101 as primary clock chip (T9_noME change 40975)
01/22/07 -- Clock Termination: Added R3051 for Silego 537/101 compatibility
01/22/07 -- BOM: Added BOMPTIONs for SLG2AP101 (primary) and SLG8LP537 (backup)
01/22/07 -- BOM: Selected P1V8S3_1V825 BOMPTION to lift voltage at FB memories
10.0.0:
01/23/07 -- BOM: Changed C3860/61 to 22pF from 27 pF based on -R characterization (T9_noME change 41248)
01/23/07 -- BOM: Changed FB memories to new Samsung and Hynix APNs (also added new BOMPTIONs to GPU straps)
01/23/07 -- Released for EVT (Schem Rev 10, PCB Rev 02)

EVT_SE

10.1.0:
01/24/07 -- PATA Conn: Added pass FET Q4430 to allow PCIREQ3 (ODD reset GPIO) to pullup to S0
01/24/07 -- PATA Conn: Changed =PP5V_S0_ODDPWREN to =PP3V3_S0_ODDPWREN for minor power savings
01/24/07 -- Power Aliases: Updated PP3V3_S0 aliases to support above changes
10.2.0:
01/25/07 -- PATA Conn: Replaced PCIREQ pass FET with OD buffer to correct a corner case during PLTRST
01/25/07 -- Power Aliases: Updated PP5V_S0 aliases to support above changes
11.0.0:
01/25/07 -- BOM: Updated gain of PP1V25_ENET current sense amplifier to 165 (R5432 to 165K)
01/25/07 -- BOM: Updated all Intel APNs to use QS parts
01/25/07 -- Released for EVT (Schem Rev 11, PCB Rev 03)
12.0.0:
02/19/07 -- GPU Reset: Changed C2885 to 0.047uF to reduce reset delay on powerup
02/19/07 -- GPU PGOOD: Changed C9595 to 330pF to reduce PGOOD delay on powerup
02/19/07 -- Power Sequencing: NO STUFFed U7885 to remove GPU PGOOD from PWROK chain
02/19/07 -- Power Sequencing Rework: Short pins 2 and 4 of U7885 to complete PWROK chain
02/19/07 -- Released post-EVT to document what was built (Schem Rev 12)

DVT

12.1.0:
02/20/07 -- GPU FB: Changed cal resistors per Nvidia PUN (R8290 to 45.3 ohm and R8291 to 24.9 ohm)
02/20/07 -- GPU FB: Changed unterminated-mode reference voltage to 40% (R8297 -> 1.02K, R8432/82, R8532/82 -> 2.21K)
02/21/07 -- FireWire: Changed to Rev C of TI FireWire MCM (APN: 338S0435)
02/21/07 -- Power Sequencing: Removed U7885/C7885 to take GFX_PGOOD out of PWR_OK chain (rdar://4974927)
02/26/07 -- GPU Vcore: NO STUFFed all PWRCTL related components (feature not to be supported)
02/26/07 -- GPU Vcore: Updated voltage setpoints to 1.000/1.070/1.125V (rdar://5021453)
02/26/07 -- SB GPIOs: Sync'd page25.csa to T9_MLB to get pullup updates
02/26/07 -- Thermal Sensors: Updated topology of EMC1033 filter caps (added C5515 next to IC, moved other caps to connectors - rdar://5025773)
12.2.0:
02/27/07 -- ODD Conn: Changed ODD power FET to FDC606P (from FDC638P) for reduced Rds(on) (rdar://4993378)
02/28/07 -- Power Aliases: Moving PP1V8_GPU FET source to PP1V8_S3 rather than PP1V8_S3_ISNS to improve power delivery to GPU (rdar://5021462)
12.3.0:
02/28/07 -- Left Clutch IC: Updated both I-PEX connectors to new APN (part update for shell plating)
02/28/07 -- NB GFX Core: Changed Vcore controller to ISL6263B (part consolidation effort between Apple/Intersil - rdar://5009109)
02/28/07 -- Power Supplies: Replaced APN 152S0511 with 152S0368 (duplicate APNs for same part - rdar://5009109)
03/01/07 -- Thermal Sensors: Updated topology of EMC1033 sensors (removed shorts, changed connector caps to 18pF)
03/01/07 -- NB GFX Decoupling/Power Aliases: Connected VCCD_CRT of NB to GND per CRT disable guidelines
12.4.0:
03/01/07 -- LVDS Connector: Changed pin 5 of connector from NC to PP3V3_SW_LCD (in case we add extra cable for power - rdar://5024882)
03/01/07 -- NB GFX Decoupling: Added R2260 (0.3 ohm, 0603) to bring ESR of regulator output cap in spec (rdar://5000272)
12.5.0:
03/02/07 -- Power/Signal Aliases: Added XW0900 to PP5V_S5 to enable layout improvements
12.6.0:
03/06/07 -- Power FETs: Changed Q7080 to RJK0301 which provides much lower Rds(on)
03/06/07 -- FireWire Ports: Changed D4260 to PDS340 for lower height
12.7.0:
03/06/07 -- FireWire Ports: Changed D4260 to PDS540 for higher current capacity
03/06/07 -- Ethernet Connector: Removed RX shorts on Ethernet MDI lines per EMC request
03/06/07 -- SB GPIOs: Changed R2514 from pulldown to pullup to correct auto power-on issue (Linda card detect GPIO)
03/06/07 -- DDR2 Regulator: Changed FB resistors to 0.1% to raise guaranteed lowest output voltage

DVT (cont'd)

12.8.0:
03/08/07 -- Thermal Sensors: Added R5515/R5516 in case low pass filter is needed for EMC1033
13.0.0:
03/12/07 -- Power Control: Corrected alias connections for 5V/3V3 S5 enable signals
13.1.0:
03/13/07 -- BOM Options: Removed HDCP BOM option from stuffing list (feature removed)
03/14/07 -- Constraints: Constrained WWAN_SIM signals to 50 ohms
03/14/07 -- Thermal Sensors/Aliases: Changed mounting pads of Th2H sensor connector to left clutch chassis gnd
13.2.0:
03/16/07 -- Thermal Sensors: Replaced EMC1033 with second EMC1043 for improved noise filtering
03/16/07 -- NB GFX: LVDS_VREFL/VREFH changed to single pin nets to prevent LVDS glitches per Intel
03/16/07 -- Yukon Power Control: Crystal caps changed to 18pF (rdar://4946795 and rdar://4945362)
13.3.0:
03/16/07 -- Thermal Sensors: Moved remote sensor U5500 to SMC SMBus "A" and S3 power rail to clear I2C addr clash
13.4.0:
03/19/07 -- Thermal Sensors: Updated U5500 power alias to indicate device should be on S3 rail
03/19/07 -- Power Control: Added U7858 to level shift PM_G2_EN from 3.42V to 5V
03/19/07 -- Power Supplies: For 1.8, 3.3 and 5V, removed VBST 0-ohm series R (rdar://5070179)
03/19/07 -- Power Supplies: For 1.8, 3.3 and 5V, increased cap size to 0603/0805 on VBST caps (rdar://5070179)
13.5.0:
03/19/07 -- Power Control: Tied all 4 5V/3.3V enables (EN1, EN2, EN3, EN5) together as part of PM_G2_EN
14.0.0:
03/20/07 -- GPU Vcore: Updated setpoints for GPU Vcore based upon Nvidia Vmin (i.e. 1.05V,1.05V,1.05V,1.125V)
03/20/07 -- FB: Changed FB VREF caps to 2x0.0047uF as required in Nvidia PUN 02736-001-v07 (which requests 1x0.01uF)
15.0.0:
03/30/07 -- SIL: Changed R5031 to 2.21K and R5032 to 9.53K to raise SIL current approx 15% (lightpipe dimmed by 20%)
03/30/07 -- Power Supply: Changed 1.05V power supply current limit to 10A from 8A (R7455 to 5.62k -- rdar://5095642)
04/03/07 -- Power Supply: Changed numerous 10K Rs to 100K for Energy Star compliance (rdar://5102118)
04/03/07 -- GPU FB: Changed FB clock termination to 242 ohms (2x121) per Nvidia PUN
04/03/07 -- CPU Vcore: Changed R7117,C7134 and R7115,R7130 for calibration improvements (rdar://5085959)
04/03/07 -- Released for DVT (BOM update)
16.0.0:
04/17/07 -- Power Sequencing: NO STUFFED U7858 and stuffed R7860 to allow SMC to drive S5 enable pins directly
04/17/07 -- Released for DVT (As-Built)

PVT

16.1.0:
04/18/07 -- GPU Misc: Added R8735-37 to implement PCI DEVID 0x407 in hardware
16.2.0:
04/18/07 -- Power FETs: Changed Q7095 to FDM6296 and pulled up to PBUS for better PP1V25_S0 FET Rds(on)
04/18/07 -- Modules: Updated Intel chipset to PRQ parts
16.3.0:
04/20/07 -- Power FETs: Changed R7097 to 220K to maintain EnergyStar compliance with FET gate pulled to PBUS
04/20/07 -- Power FETs: Changed C7095/C7083 to 16V for proper rating of parts tied to PBUS
04/20/07 -- CPU VCore: Changed C7196 to 16V to eliminate a BOM item
17.0.0:
04/20/07 -- No changes. Weekly BOM release.
A.0.0:
04/24/07 -- SB Decoupling: Changed L2700 from 155S0152 to 155S0333 for AVL updates
04/24/07 -- SMC Support: Changed R5031 to 2.37K, R5032 to 9.09K to meet SIL brightness targets
04/24/07 -- Released for PVT

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Revision History

SYNC_MASTER=N/A

SYNC_DATE=N/A

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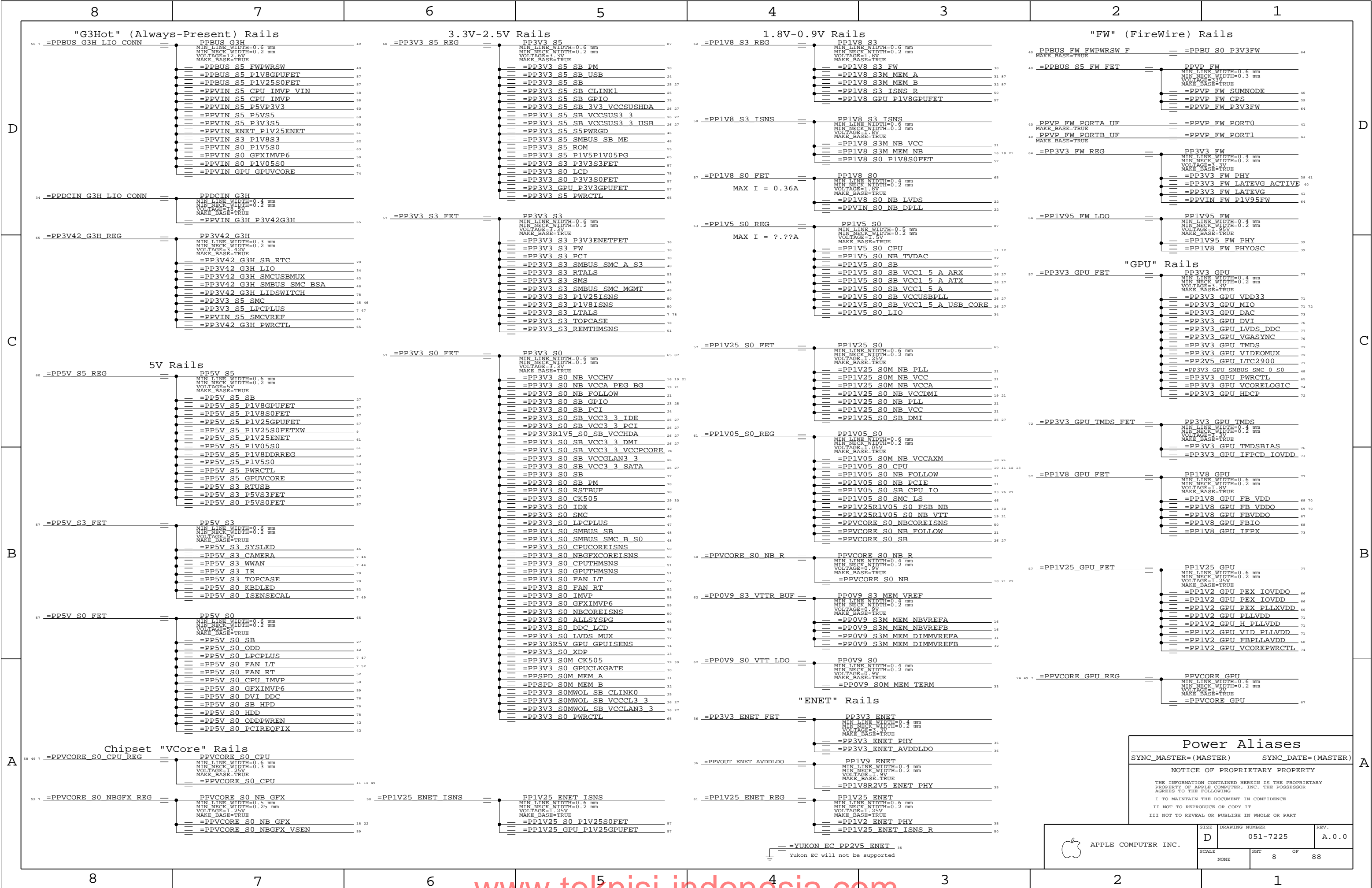
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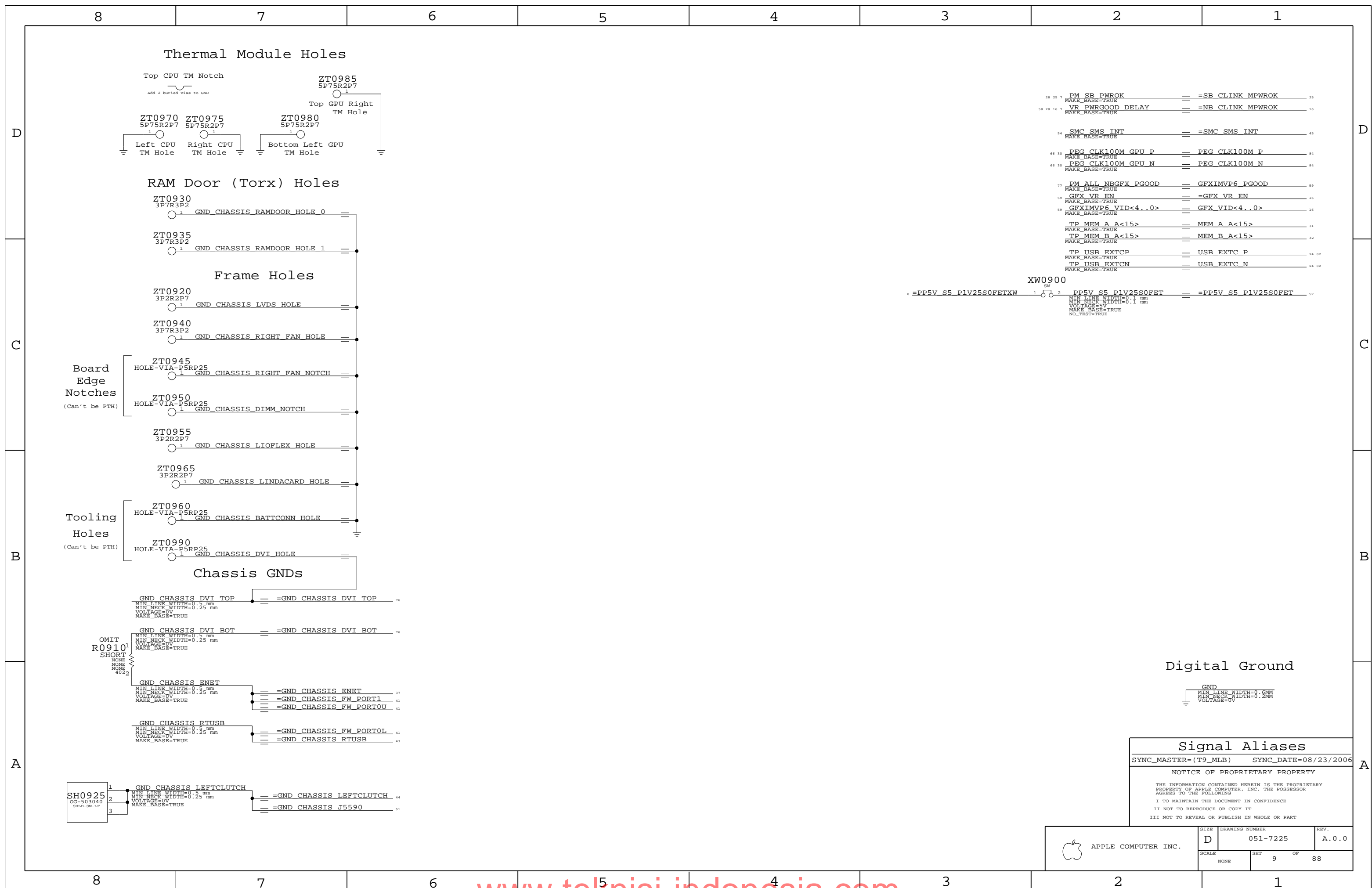
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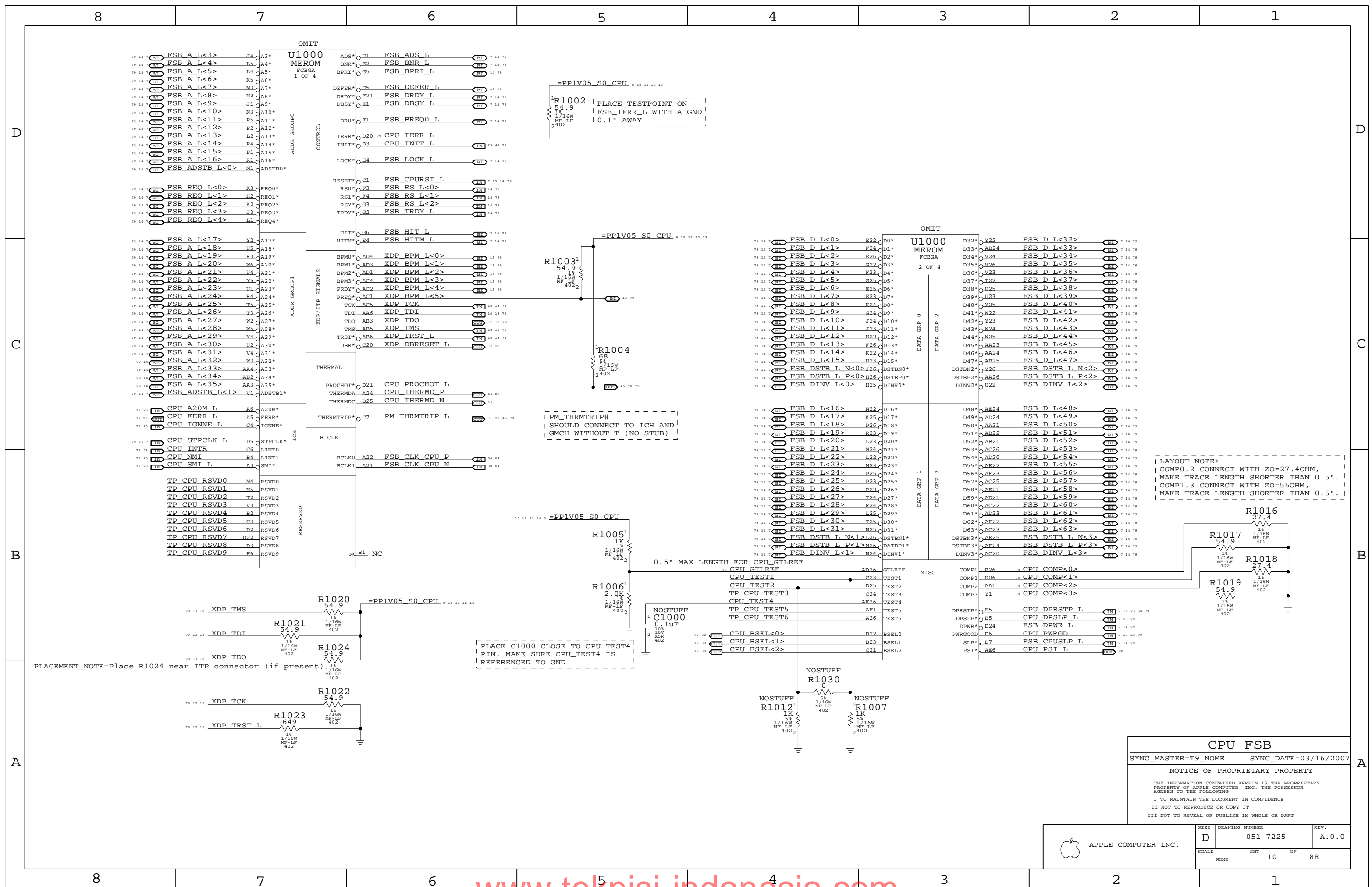
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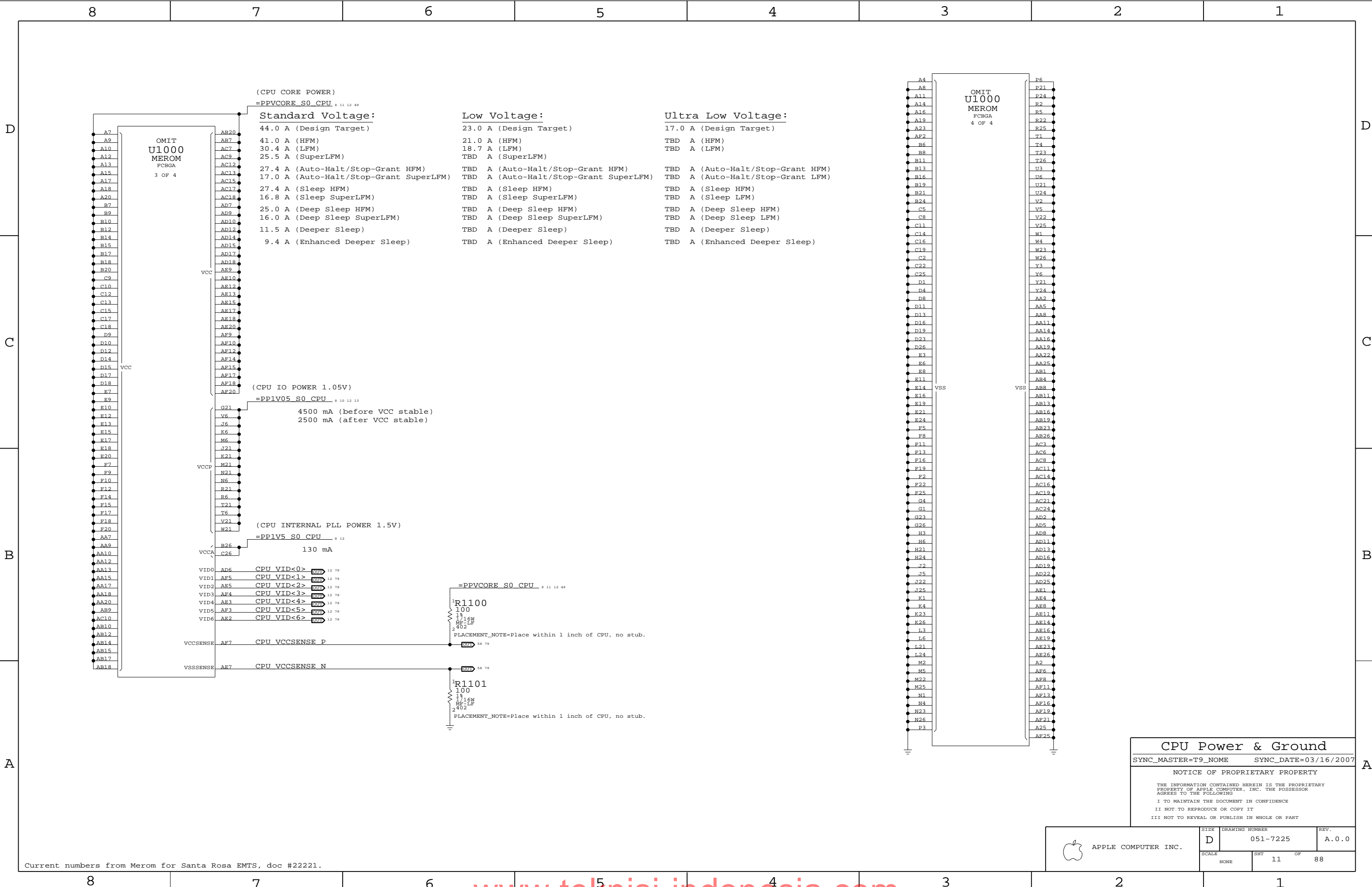
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Functional Test Points				ICT Test Points			
Fan Connectors		Battery Digital Connector		CPU FSB NO_TESTS		NB NO_TESTS	
FANC_TEST		FANC_TEST		NO_TEST		NO_TEST	
TRUE =PP5V S0 FAN LT 8 52		TRUE SMC BS ALRT L 45 46 56		TRUE FSB A L<31..3> 10 14 79		TRUE NC NB NC<1..16> TP NB NC<1..16> 16	
TRUE FAN LT PWM 52		TRUE =SMBUS BATT_SCL 48 56		TRUE FSB ADS L 10 14 79			
TRUE FAN LT TACH 52		TRUE =SMBUS BATT_SDA 48 56		TRUE FSB ADSTB L<1..0> 10 14 79			
TRUE FAN RT PWM 52		TRUE GND BATT 56		TRUE FSB BNR L 10 14 79			
TRUE FAN RT TACH 52				TRUE FSB BREQ0 L 10 14 79			
				TRUE FSB D L<63..0> 10 14 79			
				TRUE FSB DBSY L 10 14 79			
				TRUE FSB DINV L<3..0> 10 14 79			
				TRUE FSB DRDY L 10 14 79			
				TRUE FSB DSTB L N<3..0> 10 14 79			
				TRUE FSB DSTB L P<3..0> 10 14 79			
				TRUE FSB HIT L 10 14 79			
				TRUE FSB HITM L 10 14 79			
				TRUE FSB LOCK L 10 14 79			
				TRUE FSB REQ L<4..0> 10 14 79			
LPC+ Debug Connector		Left I/O Power Connector		GPU NO_TESTS			
FANC_TEST		FANC_TEST		NO_TEST			
TRUE =PP3V3 S5 LPCPLUS 8 47		TRUE =PPBUS G3H LIO CONN 8 56		LVDS L DATA N<1> 73 77 86			
TRUE =PP5V S0 LPCPLUS 8 47		TRUE GND		LVDS L DATA N<2> 73 77 86			
TRUE LPC AD<0> 23 45 47		Request for at least 10 GND test points		LVDS L DATA P<2> 73 77 86			
TRUE LPC AD<1> 23 45 47		NOTE: 10 additional GND test points are					
TRUE LPC FRAME L 23 45 47		called out separately in these notes.					
TRUE PM_CLKRUN L 25 45 47		RTC Battery Connector					
TRUE BOOT LPC SPI L 24 47		FANC_TEST					
TRUE SMC TMS 45 46 47		TRUE PPVBATT G3 RTC 28					
TRUE DEBUG RESET L 28 47		TRUE GND					
TRUE SMC TRST L 45 47							
TRUE SMC TDO 45 46 47							
TRUE SMC MD1 45 47							
TRUE SMC TX L 43 45 46 47							
TRUE FWH INIT L 47							
TRUE PCI_CLK33M LPCPLUS 30 47 84							
TRUE LPC AD<2> 23 45 47							
TRUE LPC AD<3> 23 45 47							
TRUE INT SERIRO 25 45 47							
TRUE PM_SUS_STAT L 25 45 46 47							
TRUE SMC TDI 45 46 47							
TRUE SMC TCK 45 46 47							
TRUE SMC RESET L 45 46 47							
TRUE SMC NMI 45 47							
TRUE SMC RX L 43 45 46 47							
TRUE LINDACARD GPIO 25 47							
Left ALS Connector		Current Sense Calibration					
FANC_TEST		FANC_TEST					
TRUE =PP3V3 S3 LTALS 8 78		TRUE ISENSE_CAL_EN 45 49					
TRUE ALS_GAIN 45 53 78		TRUE =PP5V S0 ISENSECAL 8 49					
TRUE LTALS_OUT 53 78		TRUE =PPVCORE S0 NBGFX_REG 8 59					
TRUE GND		TRUE =PPVCORE S0 CPU_REG 8 49 58					
		TRUE =PPVCORE GPU_REG 8 49 74					
		TRUE GND					
		6 TPs, 2 with each of above TP pairs					
Thermal Diode Connectors		Left Clutch Barrel Connector					
FANC_TEST		FANC_TEST					
TRUE HSTHMSNS D P 51 87		TRUE =PP5V S3 CAMERA 8 44					
TRUE HSTHMSNS D N 51		TRUE USB CAMERA N 24 44 82					
TRUE RSFSTHMSNS D P 51 87		TRUE USB CAMERA P 24 44 82					
TRUE RSFSTHMSNS D N 51		TRUE =PP5V S3 WWAN 8 44					
TRUE CPUTHMSNS D2 P 51 87		TRUE USB WWAN N 44					
TRUE CPUTHMSNS D2 N 51		TRUE USB WWAN P 44					
CPUTHMSNS can not be supported due to layout constraints							
System Validation TPs							
FANC_TEST		FANC_TEST					
TRUE CPU_PWRGD 10 13 23 79		TRUE IMVP_VR_ON 45 58					
TRUE CPU_DPSLP_L 7 10 23 79		TRUE IMVP_DPSRSLPVR 58 79					
TRUE PM_DPSRSLPVR 16 25 58 79		TRUE PM_SLP_S3_L 25 36 40 45 65					
TRUE CPU_DPSLP_L 7 10 23 79		TRUE PM_S4_STATE_L 25 45 65					
TRUE PM_LAN_ENABLE 25 45		TRUE PM_SLP_S5_L 25 45 46					
TRUE PCI_RST_L 24 28		TRUE PM_ENET_EN 36 65					
TRUE PM_RSMRST_L 25 45		TRUE P1V5P1V05S0_PGOOD 65					
TRUE PM_SB_PWROK 9 25 28		TRUE CPU_DPRSTP_L 10 16 23 58 79					
TRUE SB_RTC_RST_L 23 28		TRUE IMVP6_VID<6..0> 12 58 79					
TRUE PM_STPCPU_L 25 29 30		TRUE PLT_RST_L 24 28 77					
TRUE PM_STPPCI_L 25 29 30		TRUE NB_RESET_L 16 28					
TRUE VR_PWRGD_CLKEN 25 28		TRUE GPU_RESET_L 28 66					
TRUE VR_PWRGOOD_DELAY 9 16 28 58		TRUE SMC_LRESET_L 28 45					
TRUE FSB_CPURST_L 10 13 14 79		TRUE CPU_STPCLK_L 10 23 79					
TRUE FSB_CPUSLP_L 10 14 79		TRUE FSB_CLK_NB_P 14 30 84					
TRUE FSB_DPWR_L 10 14 79		TRUE FSB_CLK_NB_N 14 30 84					
TRUE NB_SB_SYNC_L 16 25		TRUE NB_CLKREQ_L 16 29					
		TRUE NB_CLK100M_PCIE_P 16 30 84					
		TRUE NB_CLK100M_PCIE_N 16 30 84					
		TRUE NB_CLK96M_DOT_P 84					
		TRUE NB_CLK96M_DOT_N 84					
		TRUE NB_CLK100M_DPLLSS_P 22 30 84					
		TRUE NB_CLK100M_DPLLSS_N 22 30 84					
		TRUE CPU_THERMTRIP_R 23					









Current numbers from Merom for Santa Rosa EMTS, doc #22221.

CPU Power & Ground

SYNC_MASTER=T9_NOME

SYNC_DATE=03/16/2007

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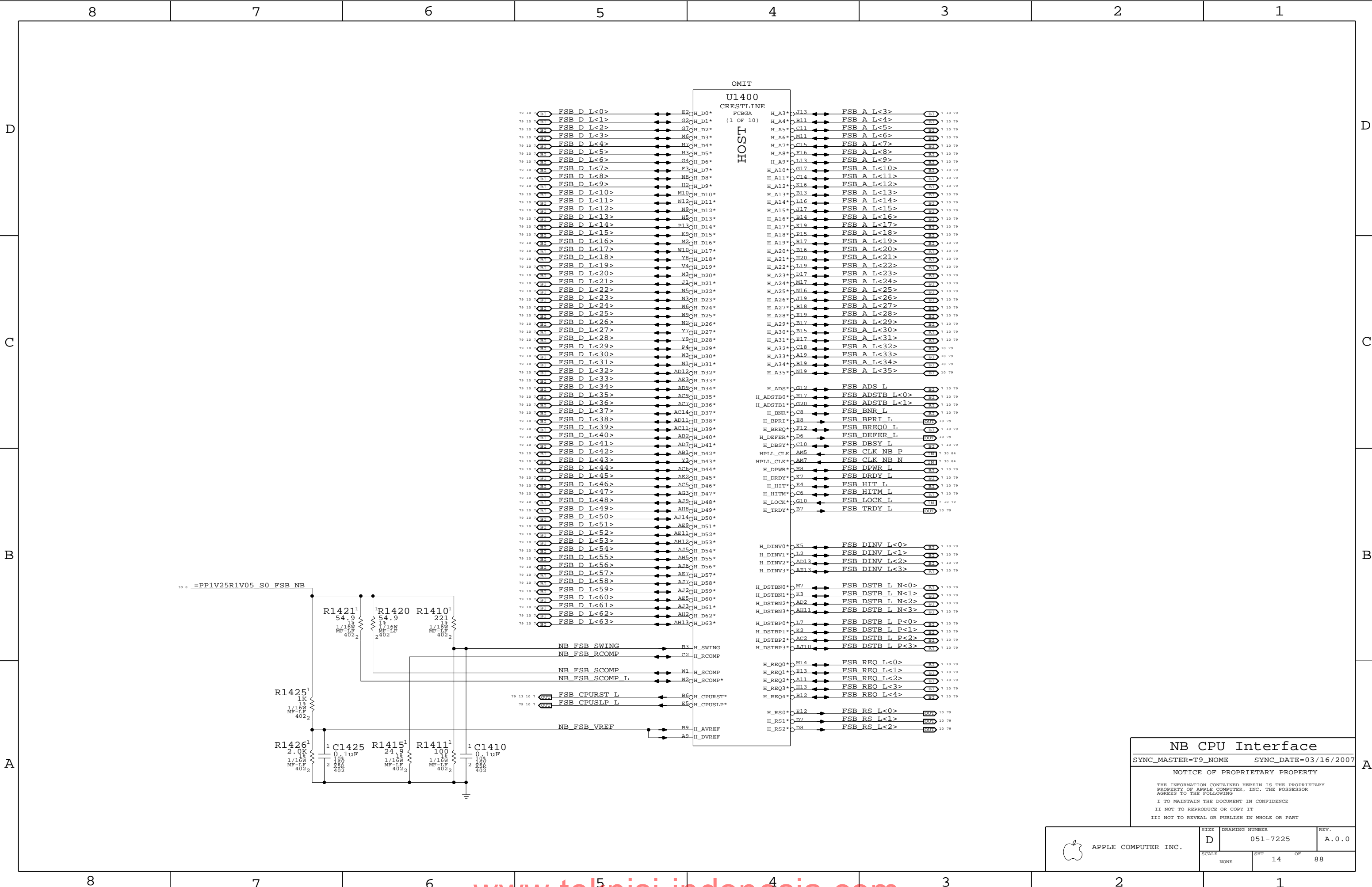
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NB CPU Interface

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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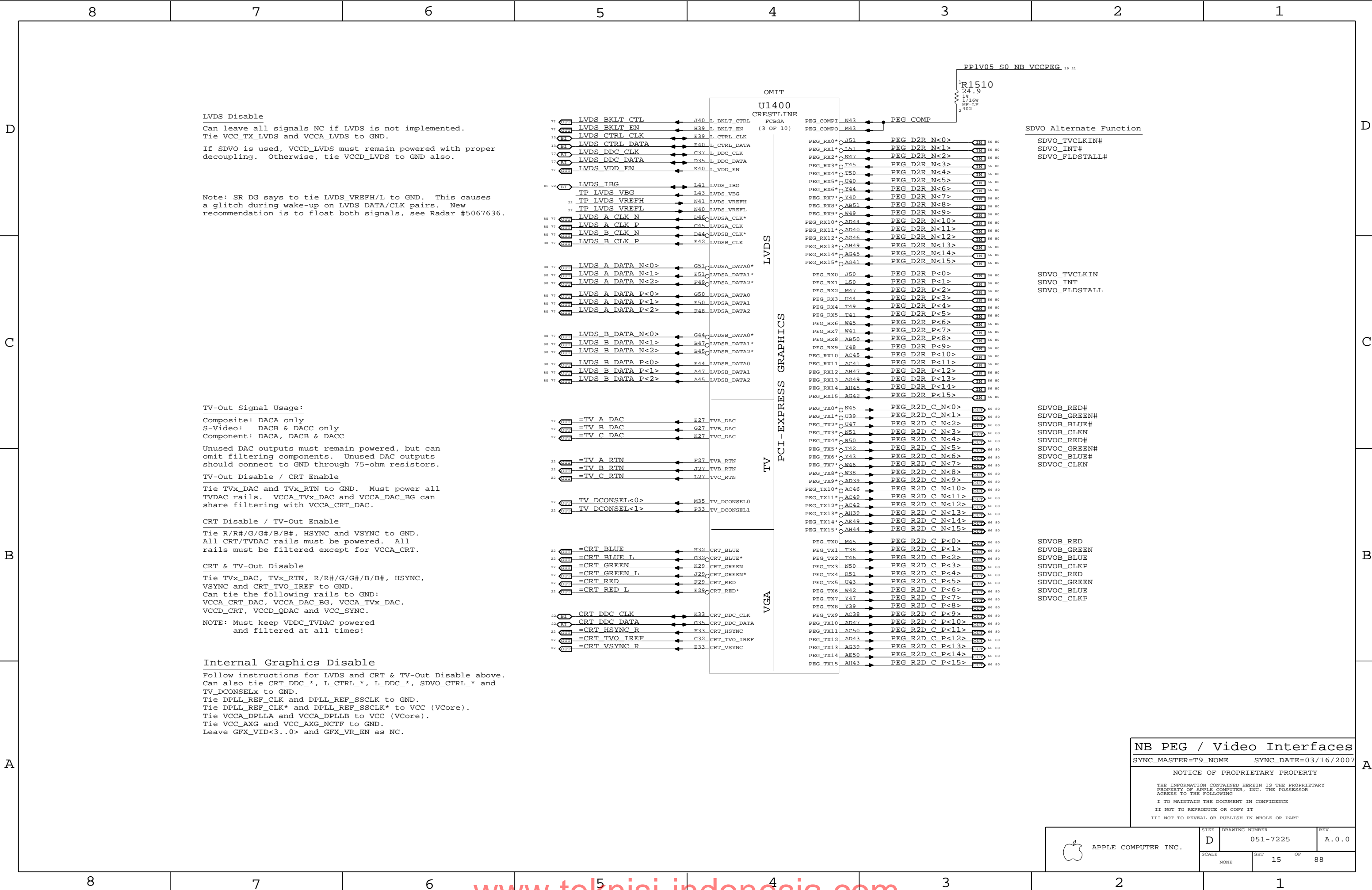
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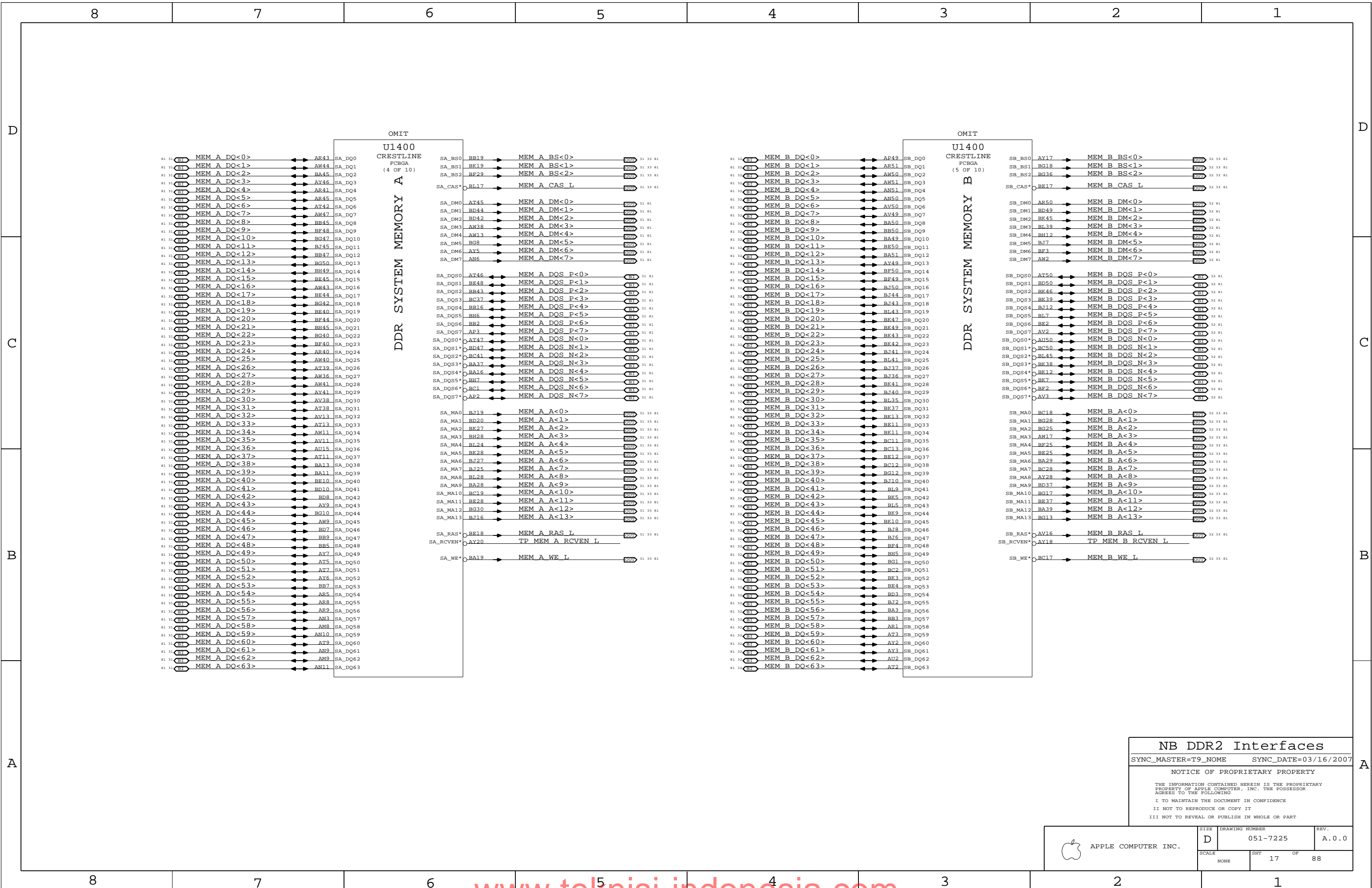
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	A.0.0
SCALE		SHT	OF
NONE		14	88







NB DDR2 Interfaces

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007


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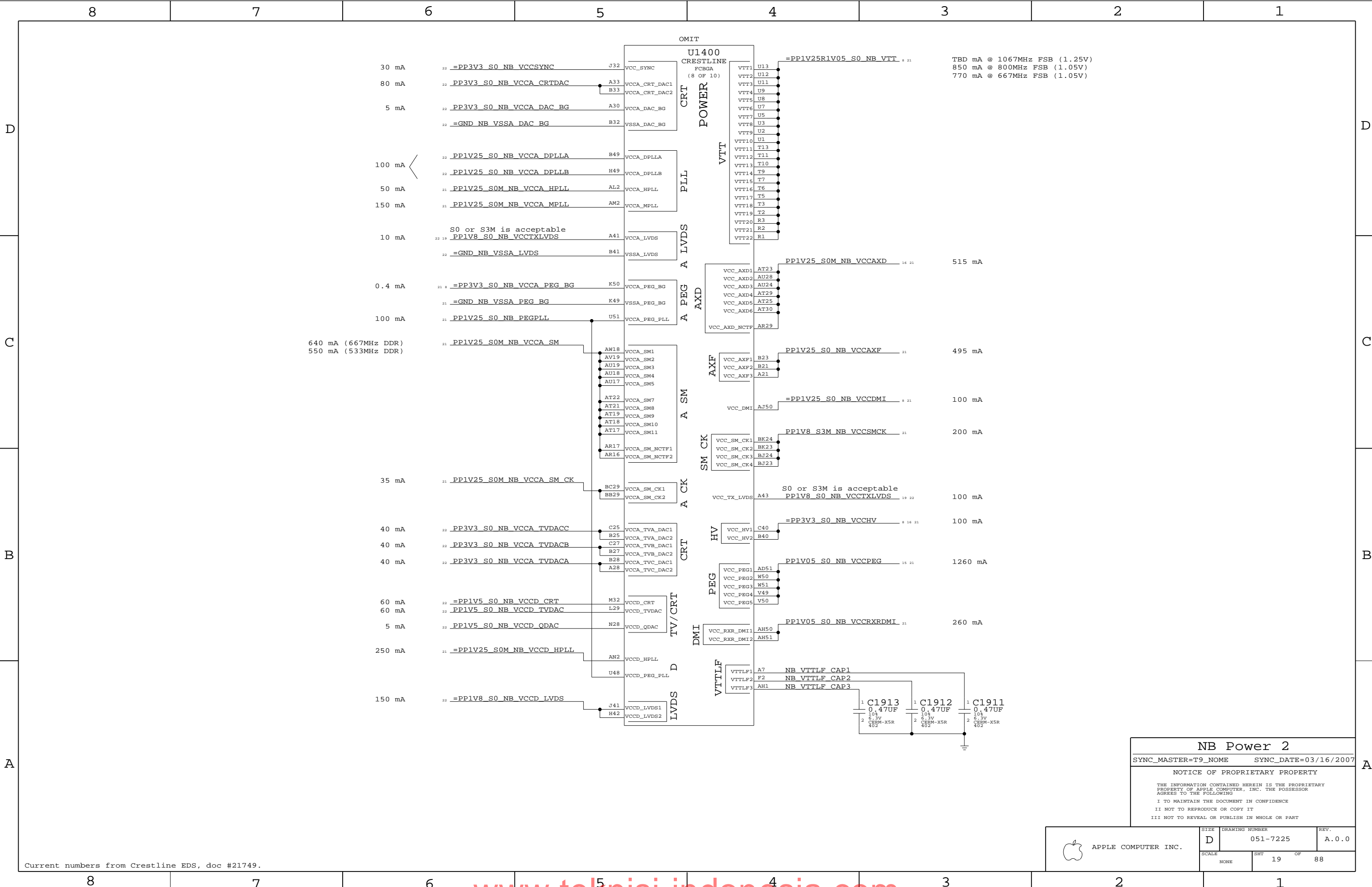
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NONE		17	88	



NB Power 2

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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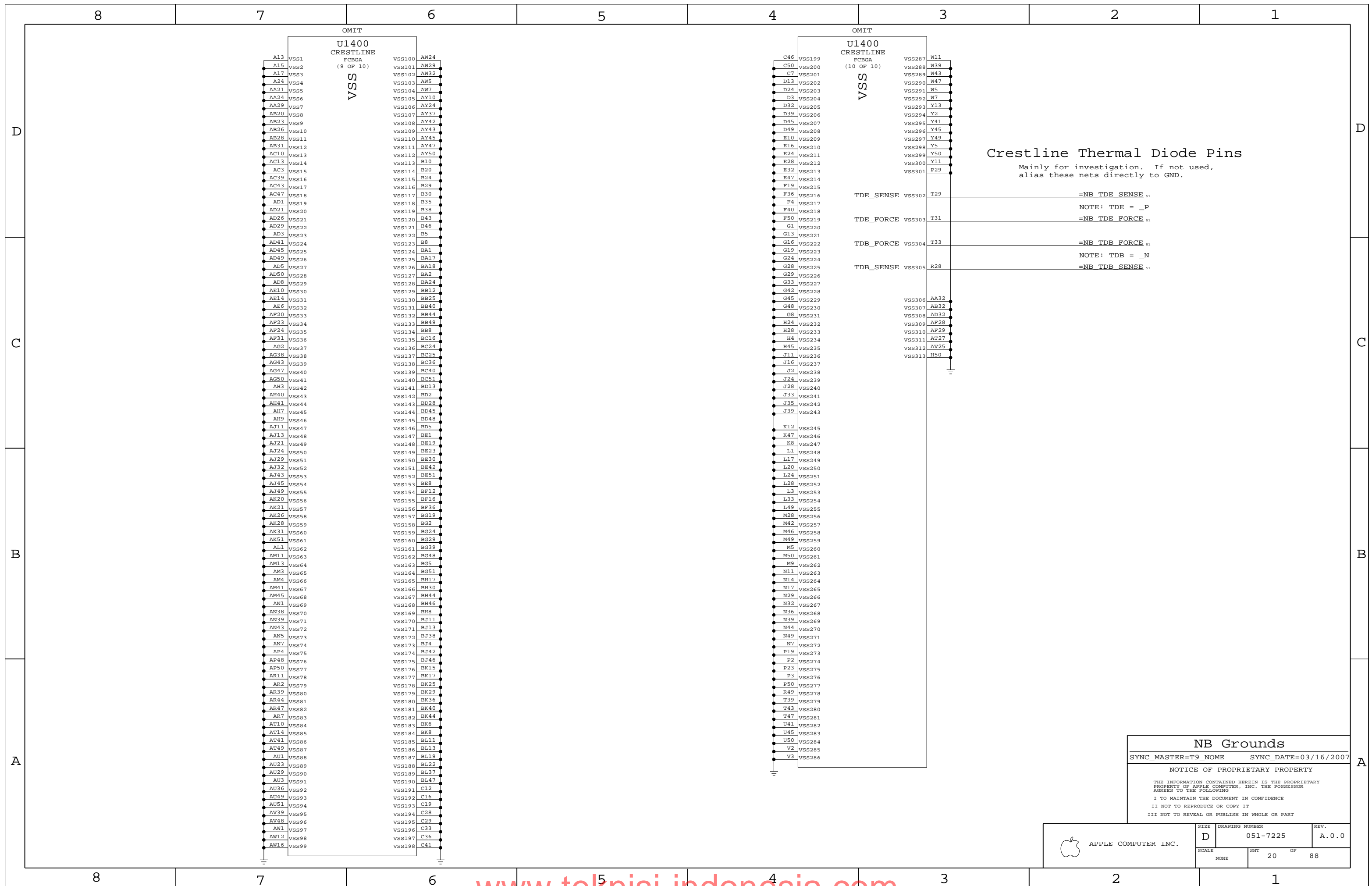
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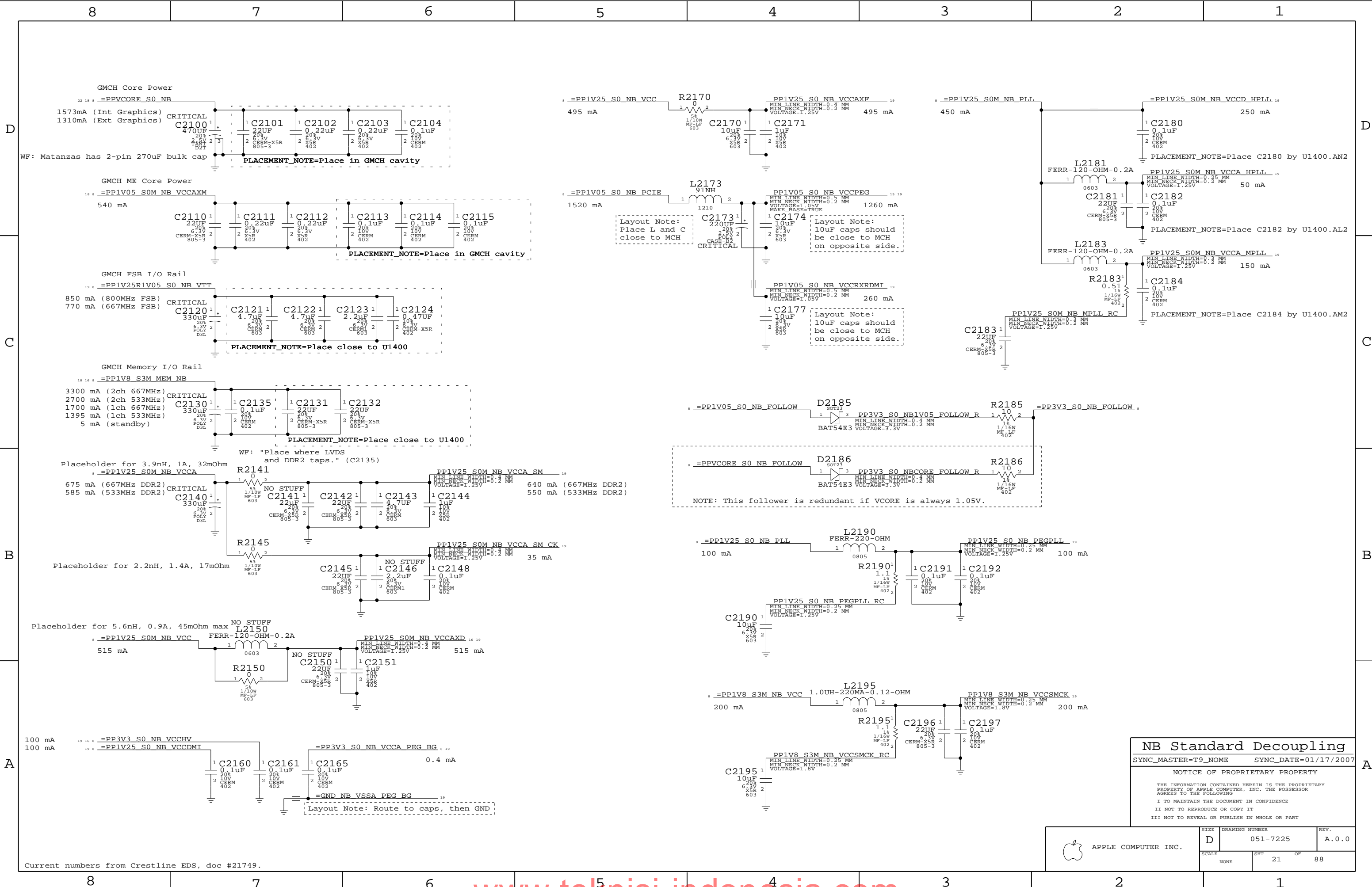
II NOT TO REPRODUCE OR COPY IT

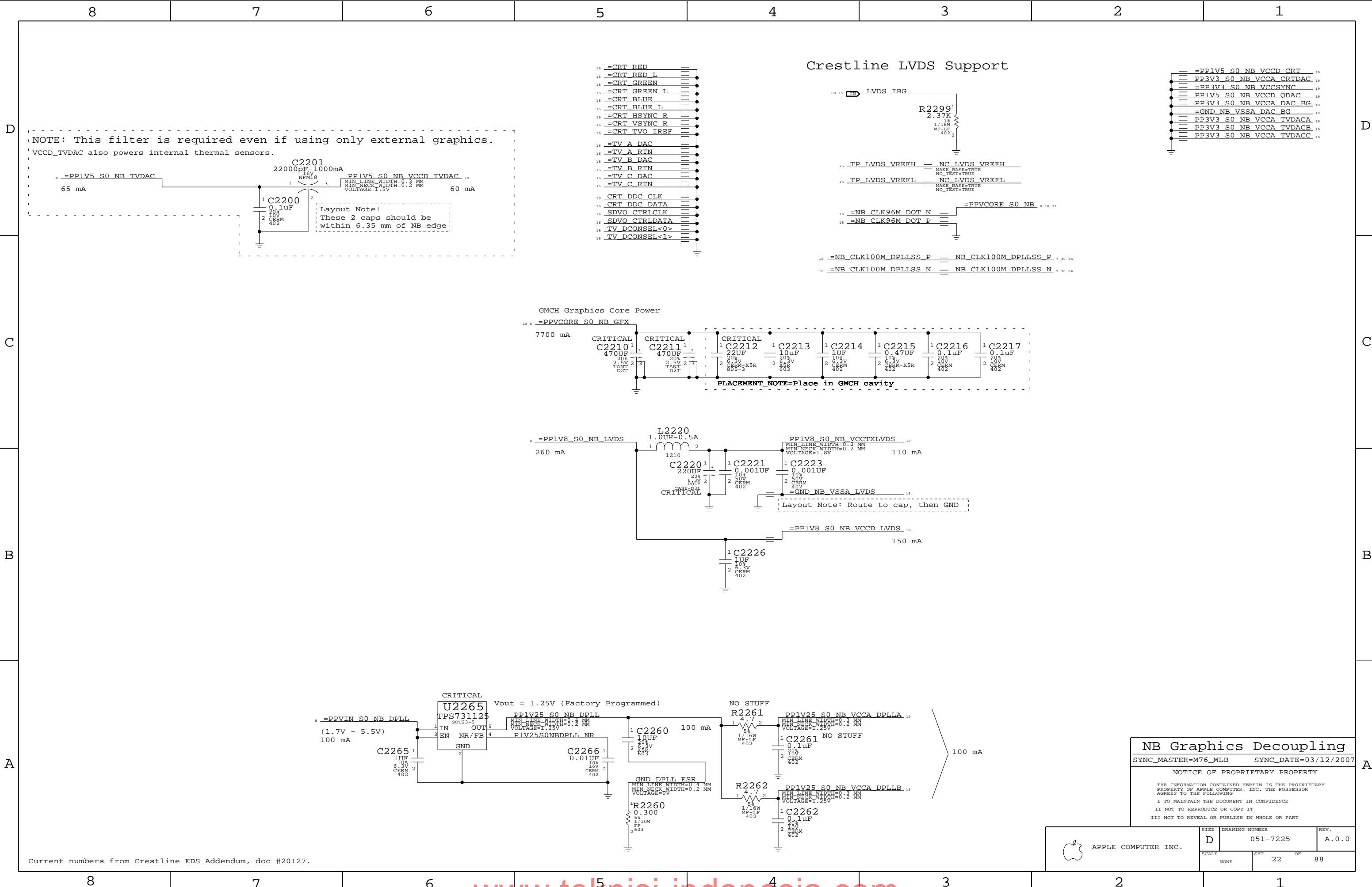
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE		SHT	OF
NONE		19	88

Current numbers from Crestline EDS, doc #21749.







NOTE: This filter is required even if using only external graphics.
VCCD_TVDAC also powers internal thermal sensors.

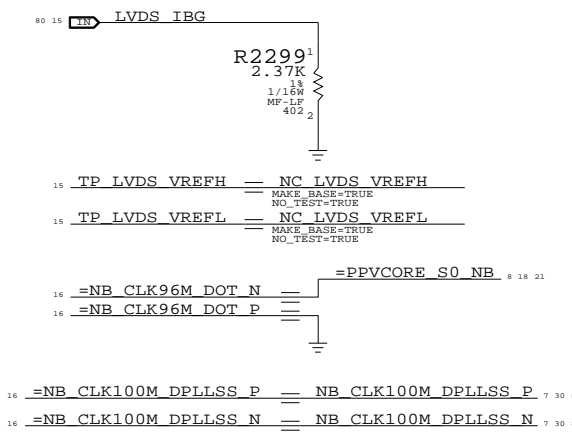
PP1V5 S0 NB TVDAC 65 mA

PP1V5 S0 NB VCCD TVDAC 60 mA

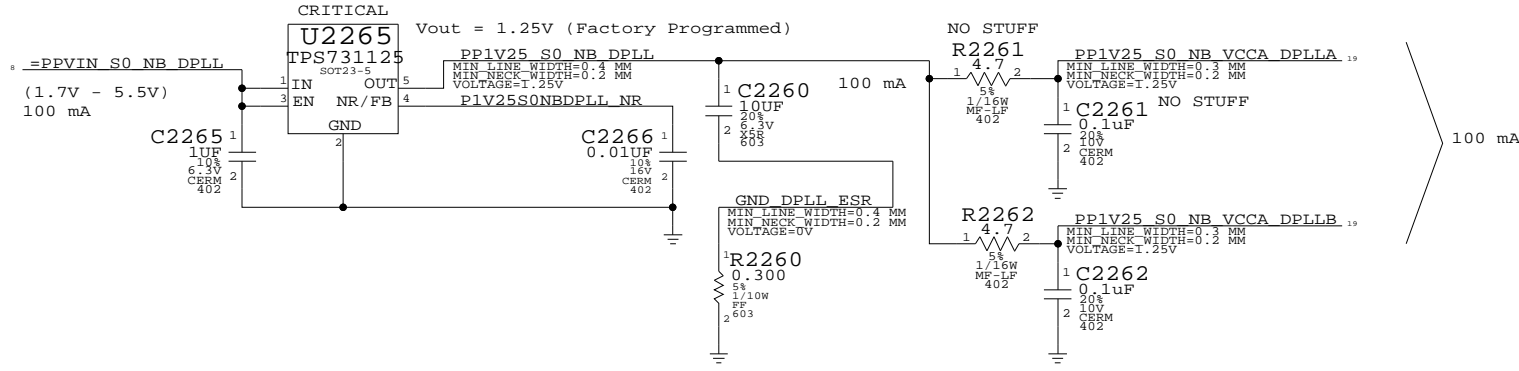
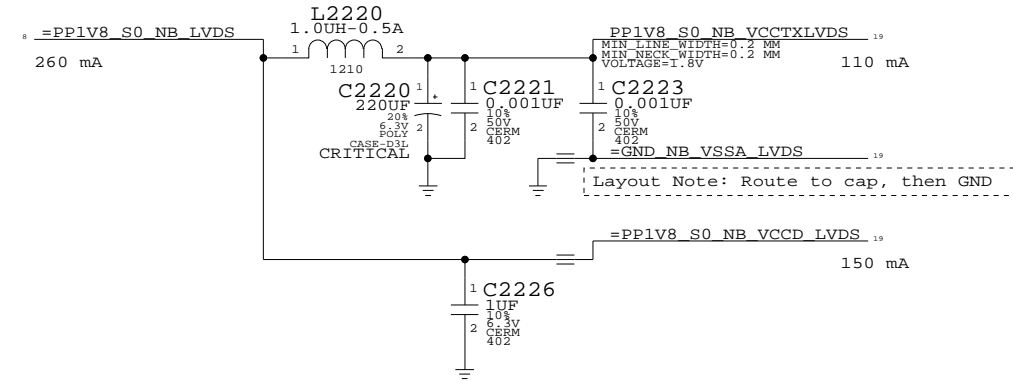
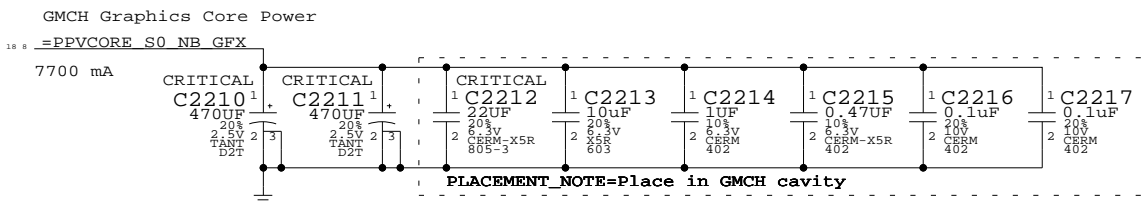
Layout Note:
These 2 caps should be within 6.35 mm of NB edge

- =CRT RED
- =CRT RED L
- =CRT GREEN
- =CRT GREEN L
- =CRT BLUE
- =CRT BLUE L
- =CRT HSYNC R
- =CRT VSYNC R
- =CRT TVO IREF
- =TV A DAC
- =TV A RTN
- =TV B DAC
- =TV B RTN
- =TV C DAC
- =TV C RTN
- CRT DDC CLK
- CRT DDC DATA
- SDVO CTRLCLK
- SDVO CTRLDATA
- TV DCONSEL<0>
- TV DCONSEL<1>

Crestline LVDS Support



- =PP1V5 S0 NB VCCD CRT
- =PP3V3 S0 NB VCCA CRTDAC
- =PP3V3 S0 NB VCCSYN
- =PP1V5 S0 NB VCCD ODAC
- =PP3V3 S0 NB VCCA DAC BG
- =GND NB VSSA DAC BG
- =PP3V3 S0 NB VCCA TVDACA
- =PP3V3 S0 NB VCCA TVDACB
- =PP3V3 S0 NB VCCA TVDACC



NB Graphics Decoupling

SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

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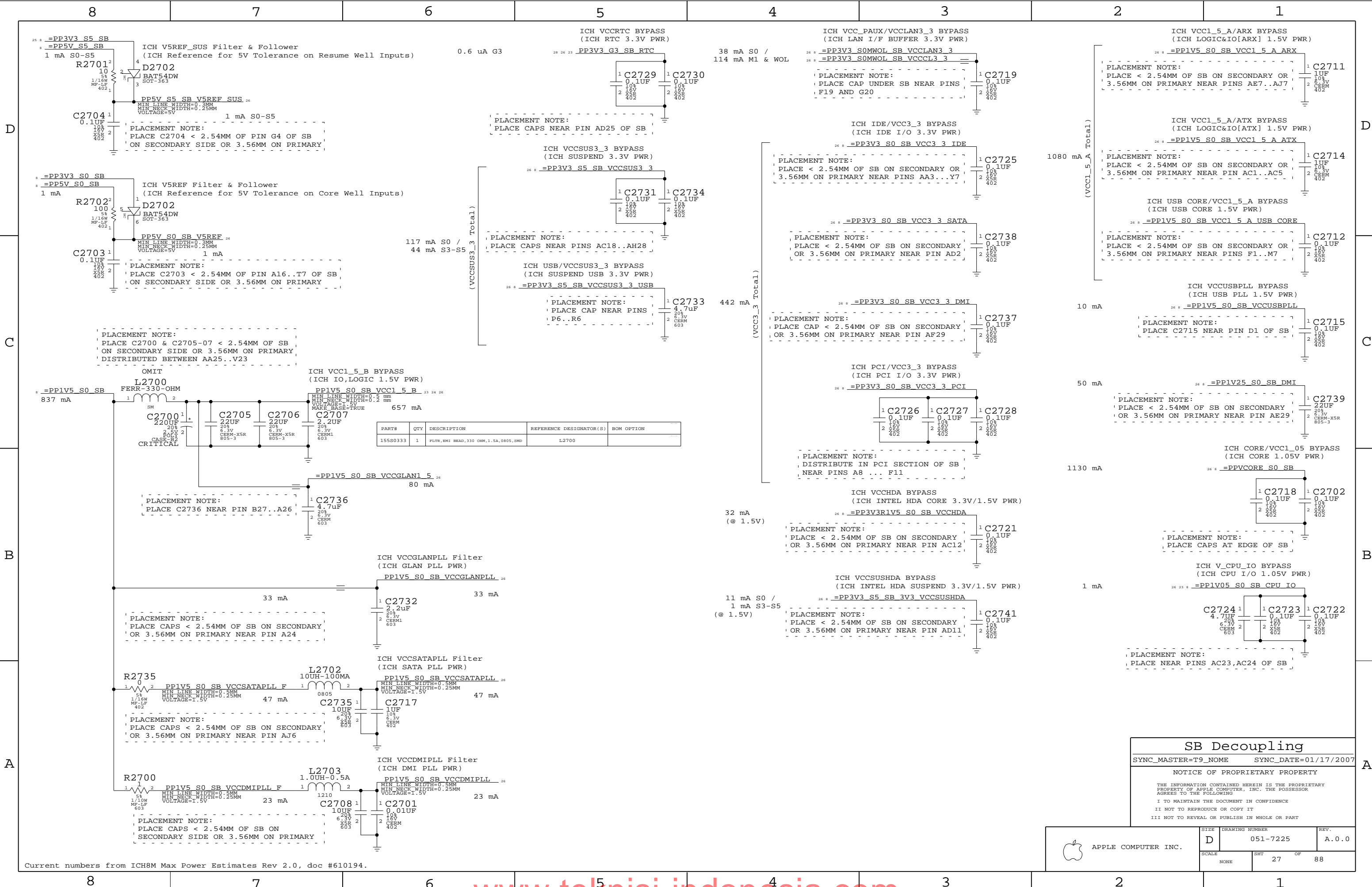
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	A.0.0
SCALE		SHT	OF
NONE		22	88

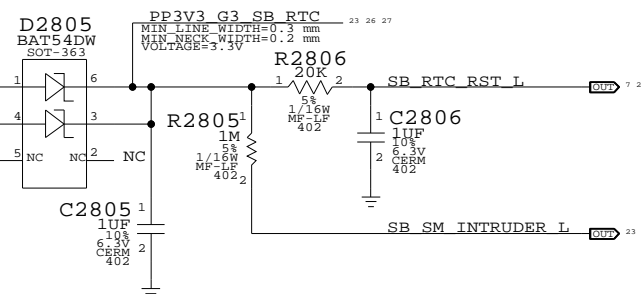
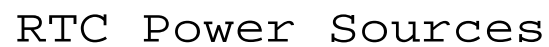
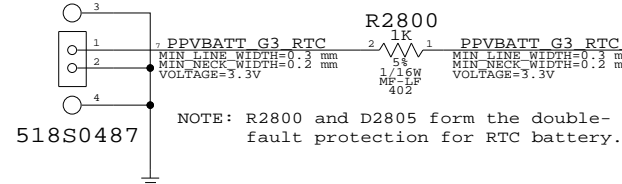
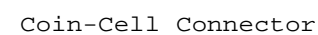
Current numbers from Crestline EDS Addendum, doc #20127.



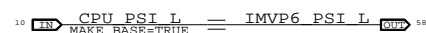
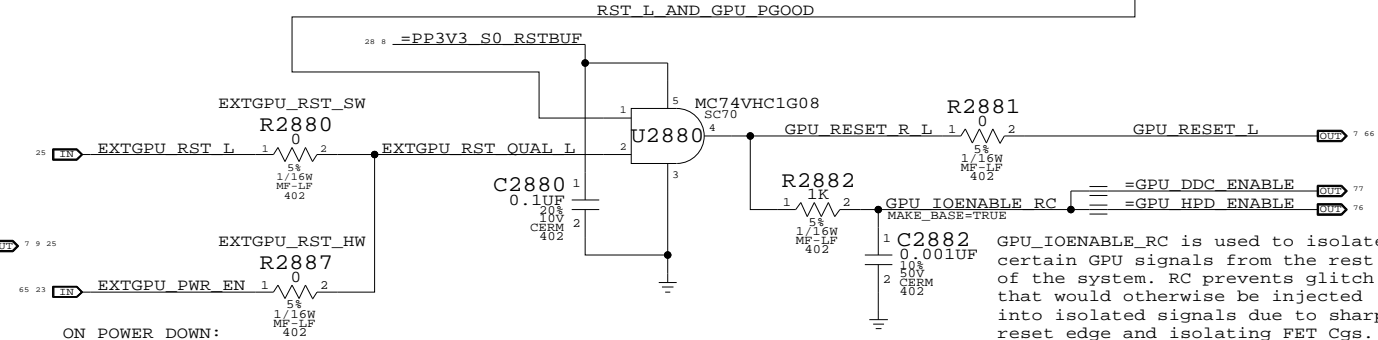
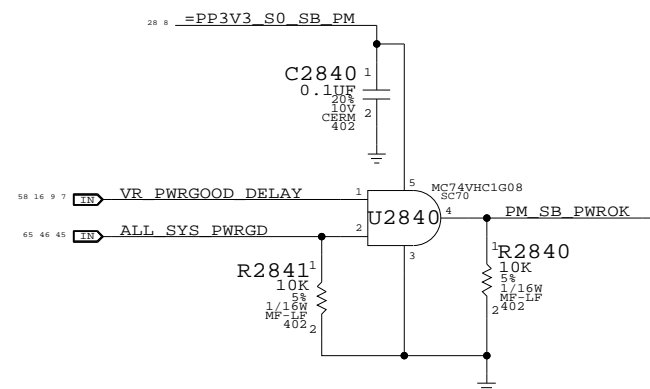
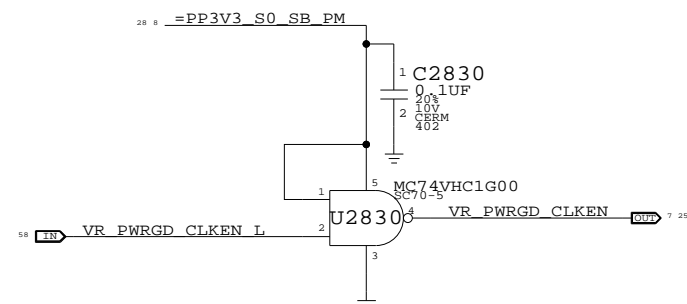
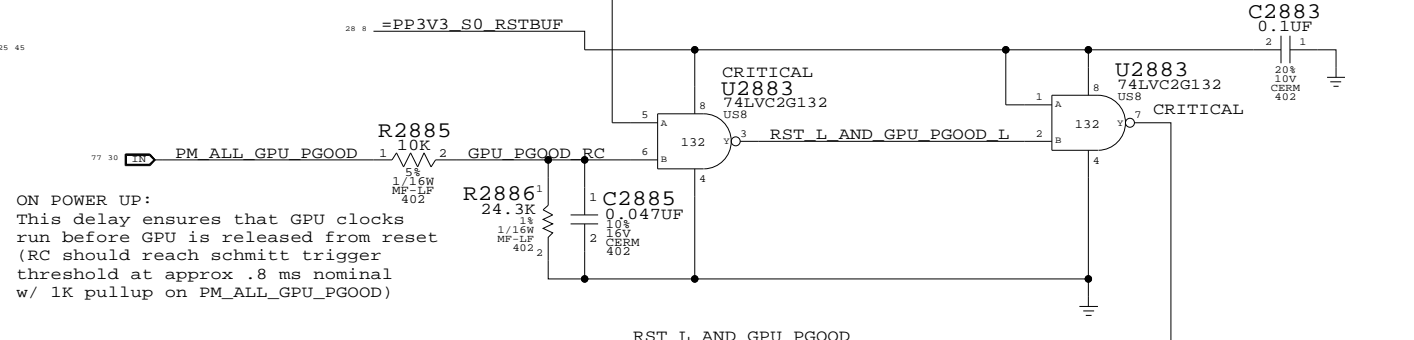
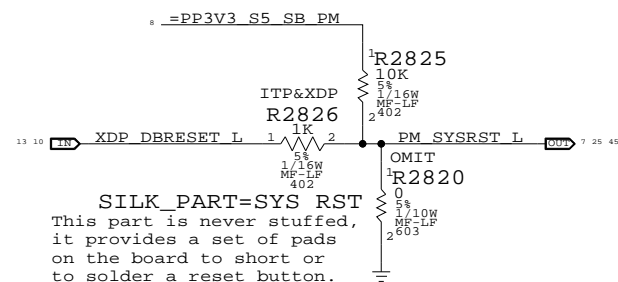
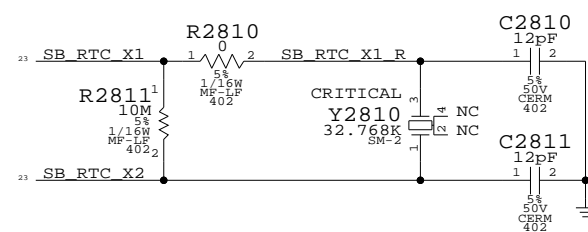
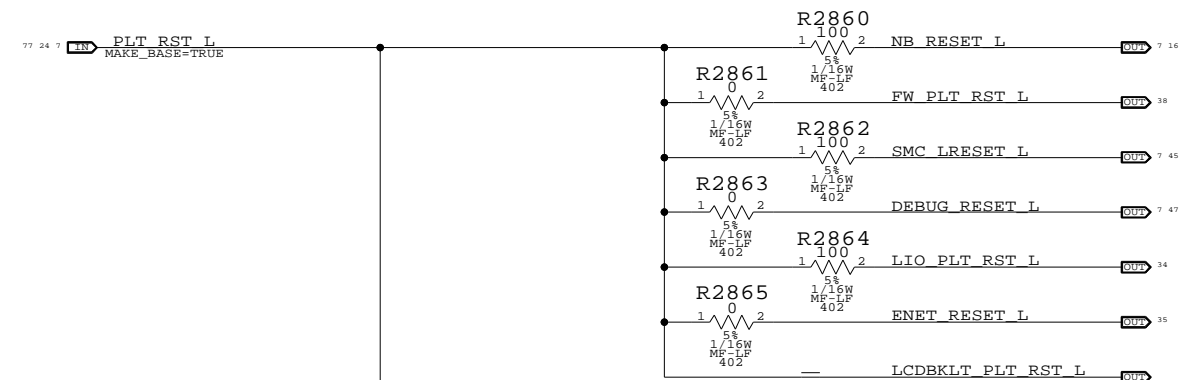








Unbuffered



SB Misc

SYNC_MASTER= (T9_MLB)	SYNC_DATE=08/24/2006
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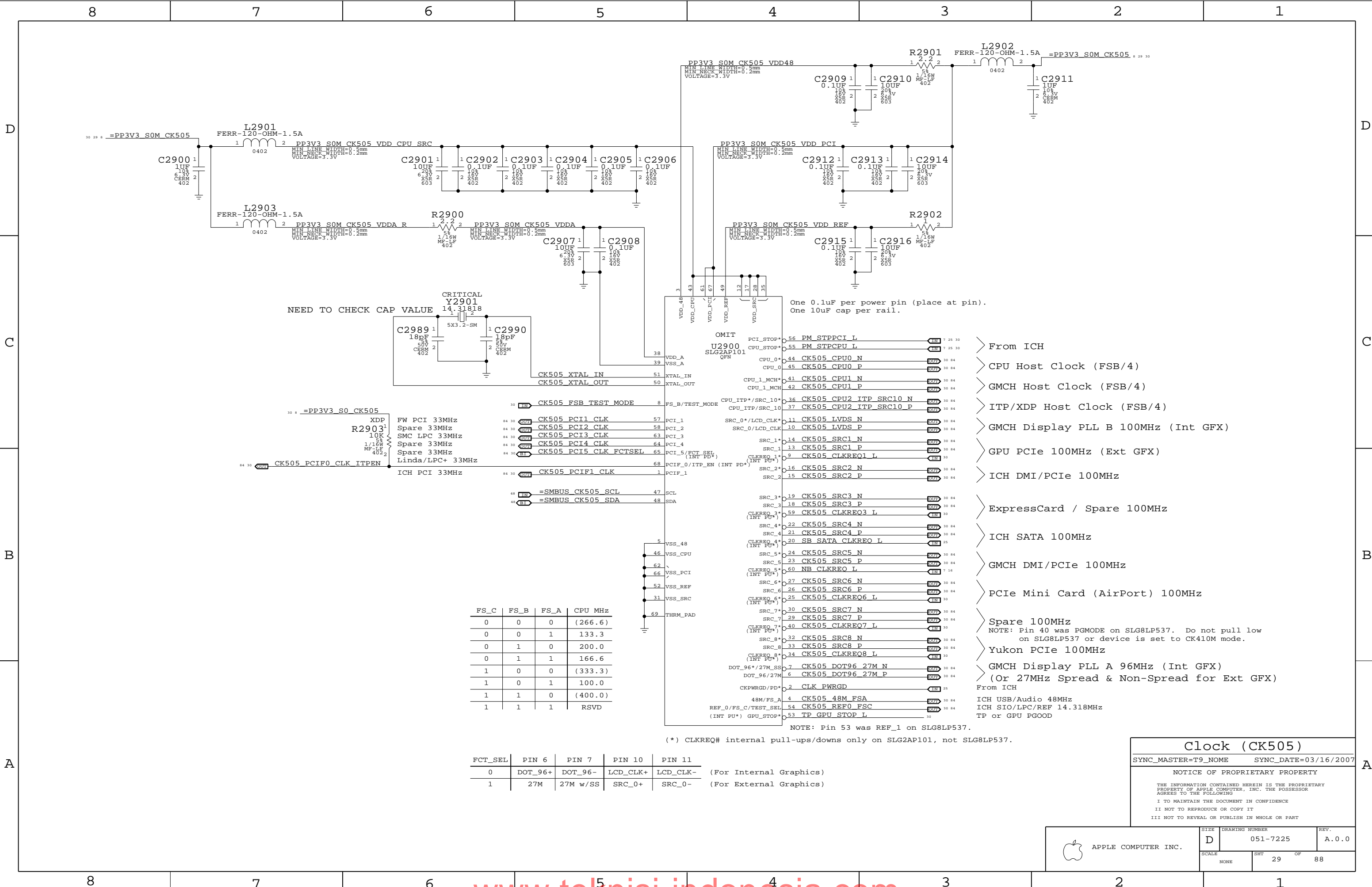
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SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0
SCALE	SHT	OF
NONE	28	88



FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-
1	27M	27M w/SS	SRC_0+	SRC_0-

(For Internal Graphics)
(For External Graphics)

Clock (CK505)

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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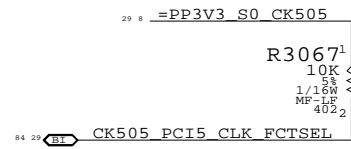
APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7225 REV. A.0.0

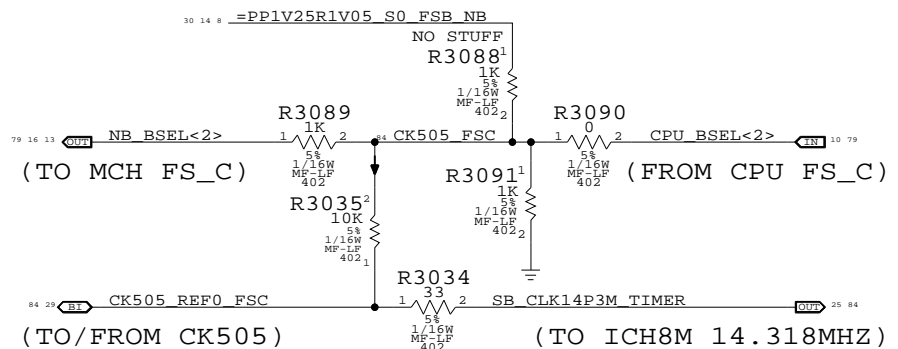
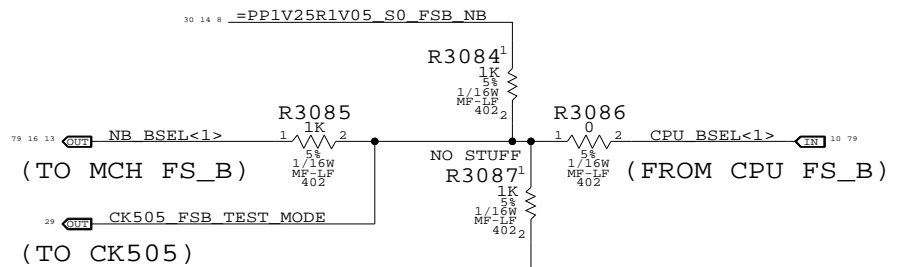
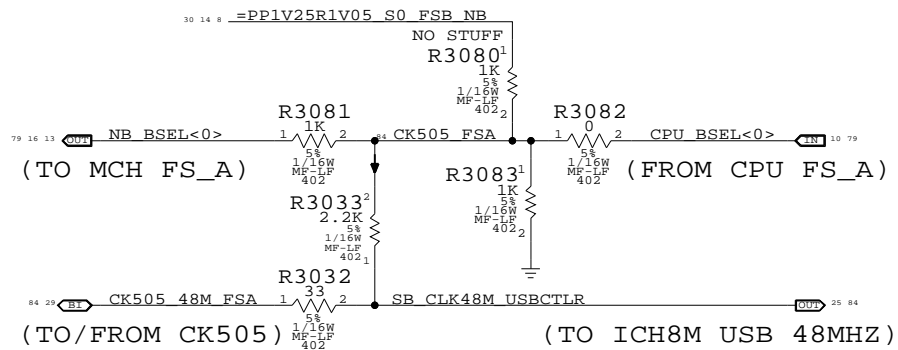
SCALE NONE SHT 29 OF 88

CK505 Configuration Straps

FCT_SEL (GFX clock select)



FS_A, FS_B, FS_C (Host clock freq select)



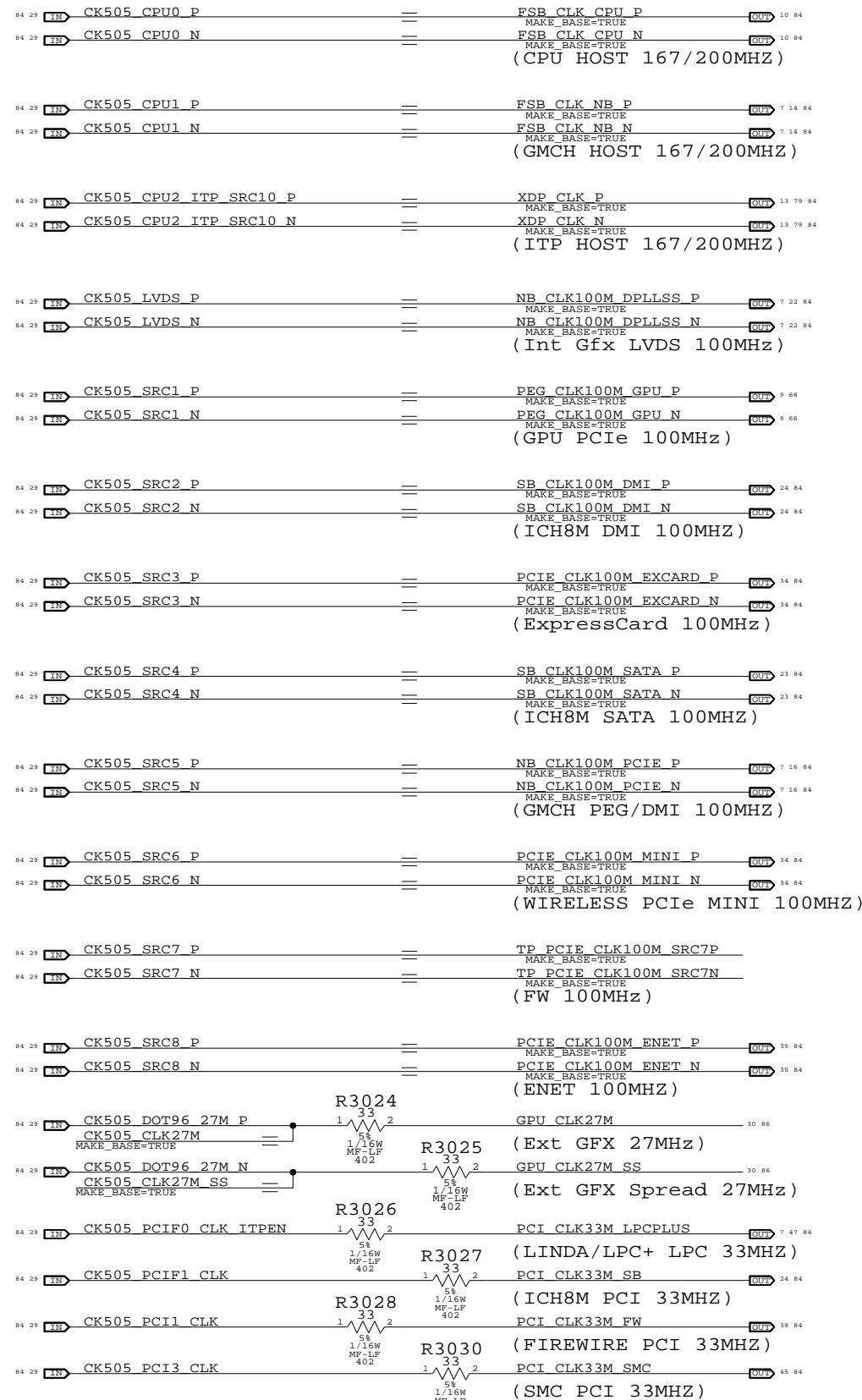
FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090 for manual CPU clk frequency.

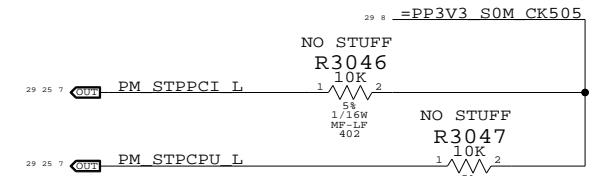
(Only 100-200MHz supported by SLG8LP536 and CY28545-5)

CLK Termination

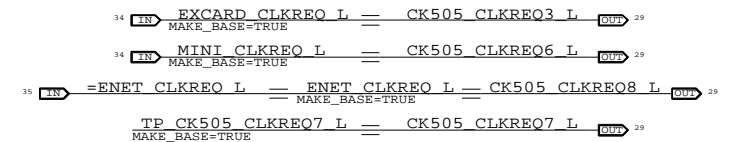
(Note: HOST/SRC/GFX clock termination removed. Silago SL8GLP536 or equiv. support only)



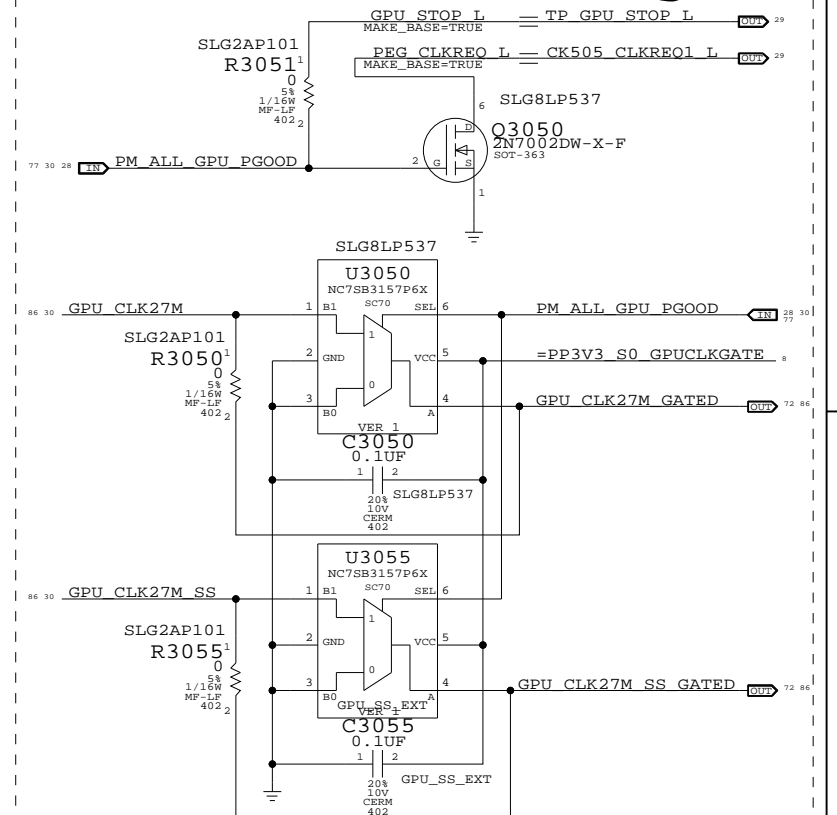
CLKREQ Controls



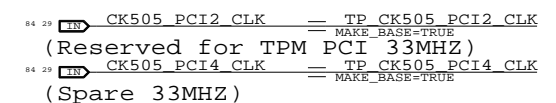
Silego SLG2AP101 has internal pull-ups on all CLKREQ# pins. Support for SL8GLP537 or equiv. only. NB and SATA CLKREQs are not remappable (and thus are not shown here).



GPU Clock Gating



Unused Clocks



Clock Termination

SYNC_MASTER=(MASTER) SYNC_DATE=08/23/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0
SCALE	SHT	OF
NONE	30	88

Page Notes

Power aliases required by this page:

- =PP1V8_S3M_MEM_A
- =PP0V9_S3M_MEM_DIMMVREFA
- =PPSPD_S0M_MEM_A (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

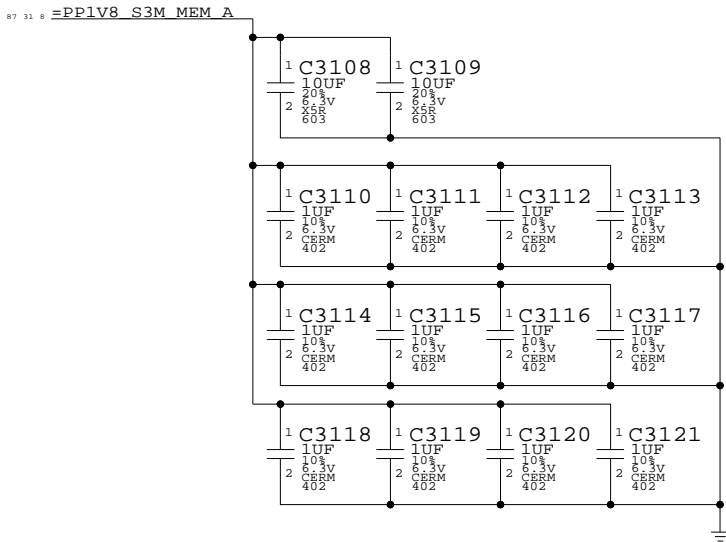
BOM options provided by this page:

(NONE)

"Factory" (thru-hole) slot

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7225

REV.

A.0.0

SCALE

NONE

SHT

31

OF

88

Page Notes

Power aliases required by this page:

- =PP1V8_S3M_MEM_B
- =PP0V9_S3M_MEM_DIMMVREFB
- =PPSPD_S0M_MEM_B (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

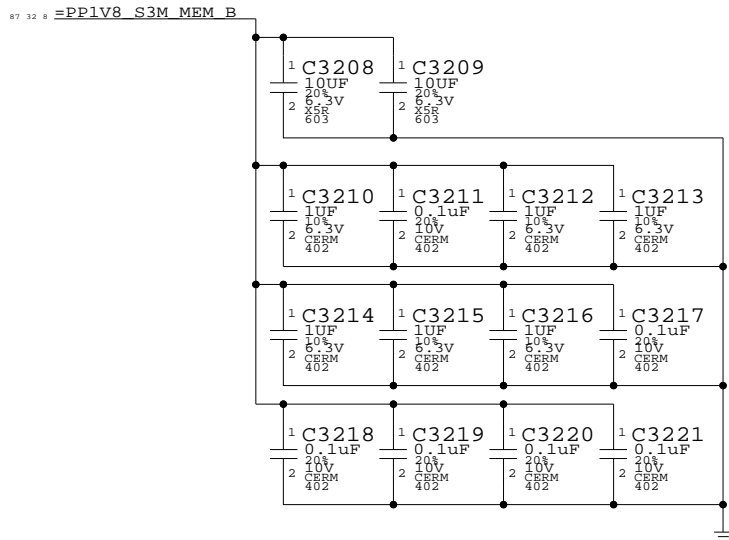
BOM options provided by this page:

(NONE)

"Expansion" (surface-mount) slot

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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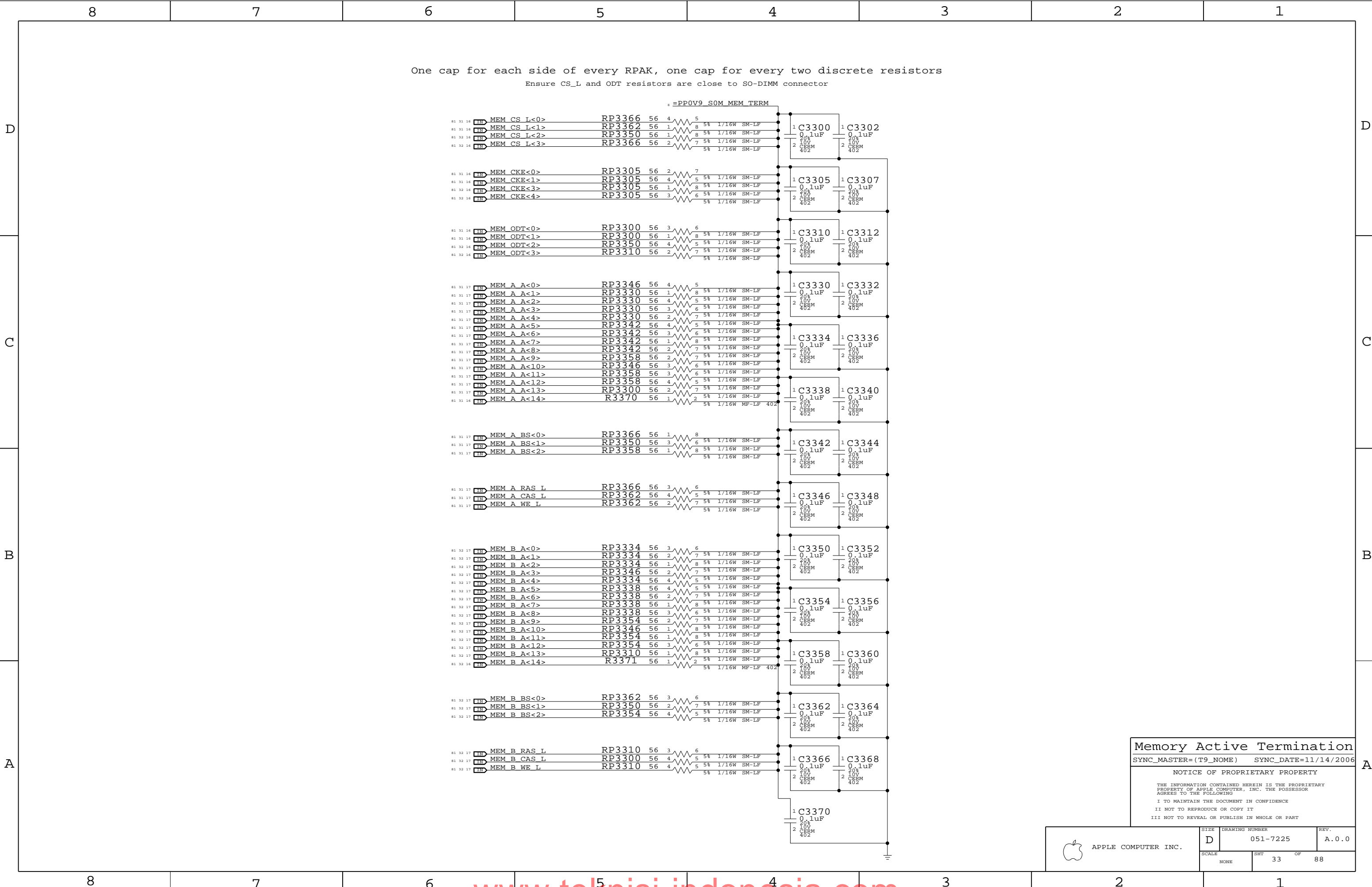
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SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0
SCALE	SHT	OF
NONE	32	88



Memory Active Termination

SYNC_MASTER=(T9_NOME) SYNC_DATE=11/14/2006

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SIZE

D

SCALE

NONE

DRAWING NUMBER

051-7225

SHT

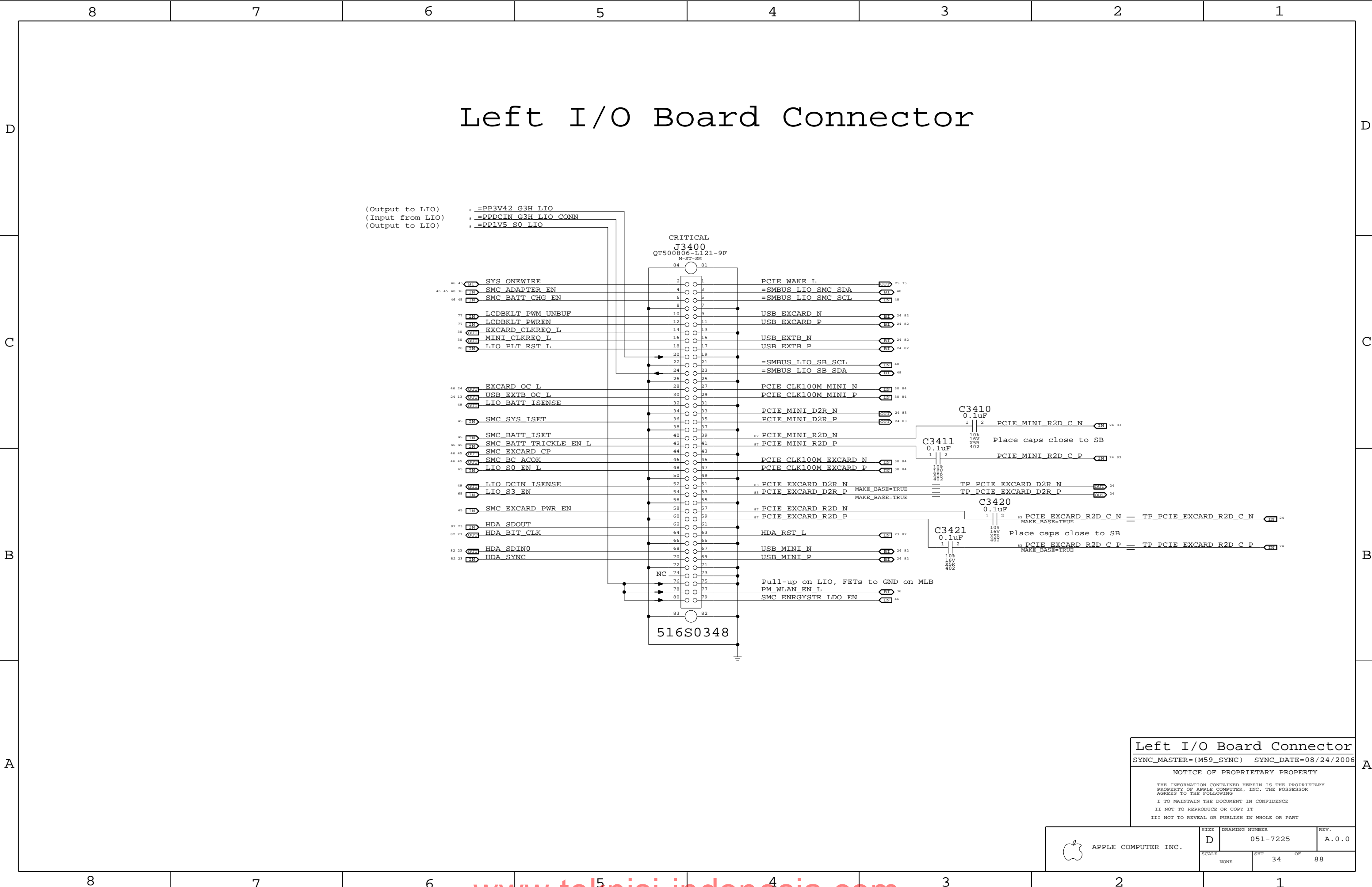
33

REV.

A.0.0

OF

88



Left I/O Board Connector

(Output to LIO)
(Input from LIO)
(Output to LIO)

=PP3V42_G3H_LIO
=PPDCIN_G3H_LIO_CONN
=PP1V5_S0_LIO

CRITICAL
J3400
QT500806-L121-9F
M-ST-SM

516S0348

Left I/O Board Connector

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

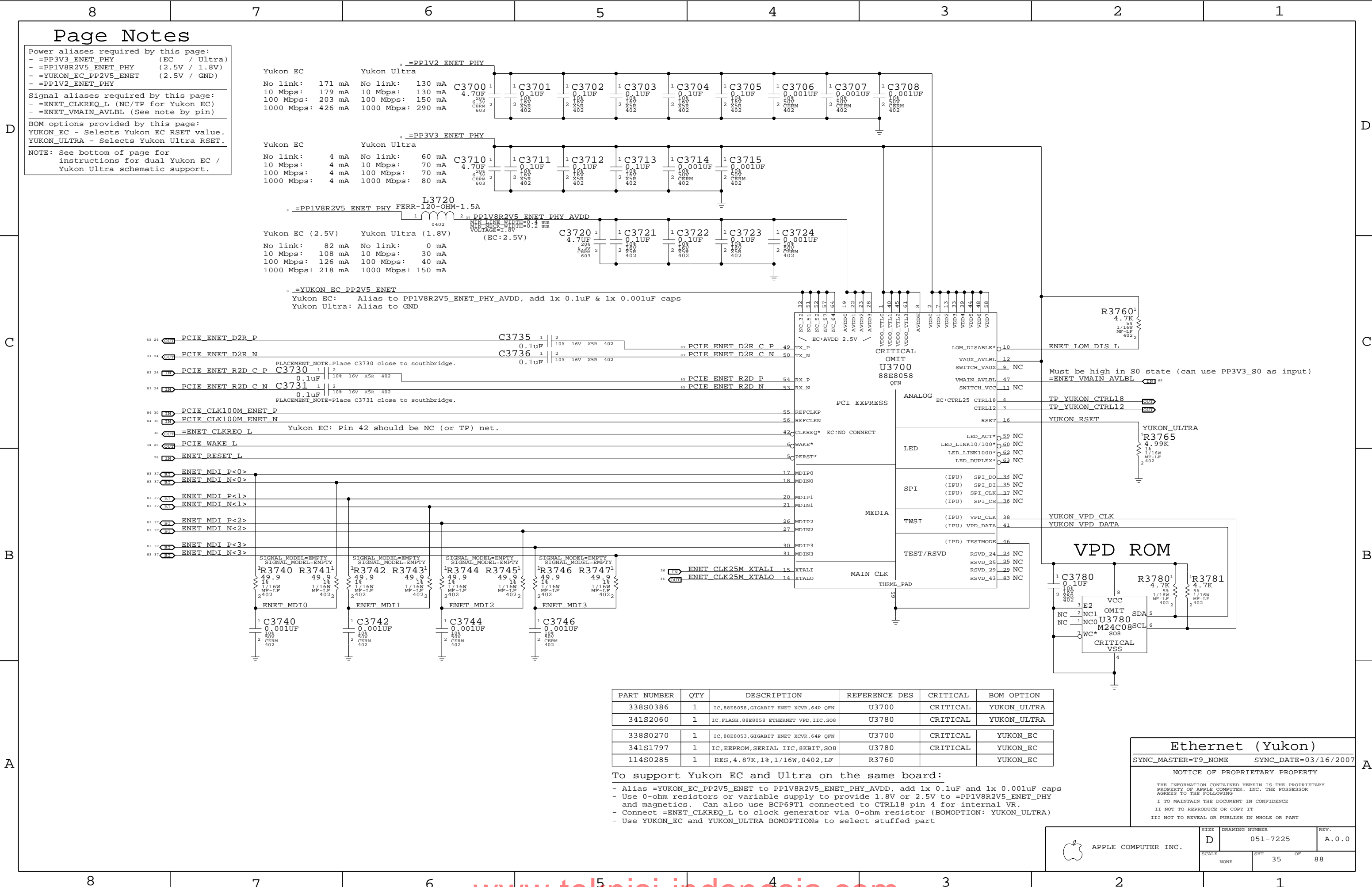
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SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0
SCALE	SHT	OF
NONE	34	88



Page Notes

Power aliases required by this page:
- =PP3V3_ENET_PHY (EC / Ultra)
- =PP1V8R2V5_ENET_PHY (2.5V / 1.8V)
- =YUKON_EC_PP2V5_ENET (2.5V / GND)
- =PP1V2_ENET_PHY

Signal aliases required by this page:
- =ENET_CLKREQ_L (NC/TP for Yukon EC)
- =ENET_VMAIN_AVLBL (See note by pin)

BOM options provided by this page:
YUKON_EC - Selects Yukon EC RSET value.
YUKON_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.

		=PP1V2_ENET_PHY	
Yukon EC	Yukon Ultra		
No link:	No link:	171 mA	130 mA
10 Mbps:	10 Mbps:	179 mA	130 mA
100 Mbps:	100 Mbps:	203 mA	150 mA
1000 Mbps:	1000 Mbps:	426 mA	290 mA

		=PP3V3_ENET_PHY	
Yukon EC	Yukon Ultra		
No link:	No link:	4 mA	60 mA
10 Mbps:	10 Mbps:	4 mA	70 mA
100 Mbps:	100 Mbps:	4 mA	70 mA
1000 Mbps:	1000 Mbps:	4 mA	80 mA

		=PP1V8R2V5_ENET_PHY FERR-120-OHM-1.5A	
Yukon EC (2.5V)	Yukon Ultra (1.8V)		
No link:	No link:	82 mA	0 mA
10 Mbps:	10 Mbps:	108 mA	30 mA
100 Mbps:	100 Mbps:	126 mA	40 mA
1000 Mbps:	1000 Mbps:	218 mA	150 mA

=YUKON_EC_PP2V5_ENET
Yukon EC: Alias to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF & 1x 0.001uF caps
Yukon Ultra: Alias to GND

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC, 88E8058, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC, FLASH, 88E8058 ETHERNET VPD, IIC, SO8	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC, 88E8053, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, SO8	U3780	CRITICAL	YUKON_EC
114S0285	1	RES, 4.87K, 1%, 1/16W, 0402, LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:

- Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONS to select stuffed part

Ethernet (Yukon)

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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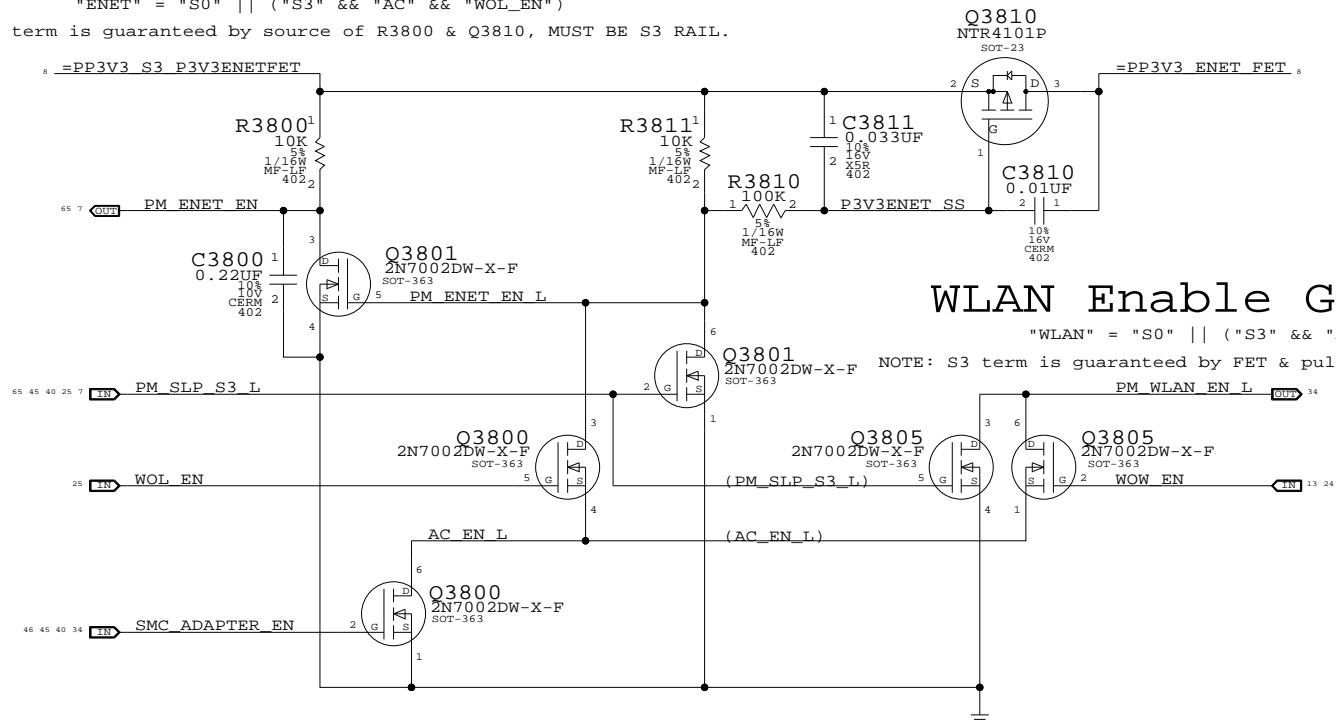
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	D	051-7225	A.0.0
SCALE		SHT	OF
NONE		35	88

ENET Enable Generation

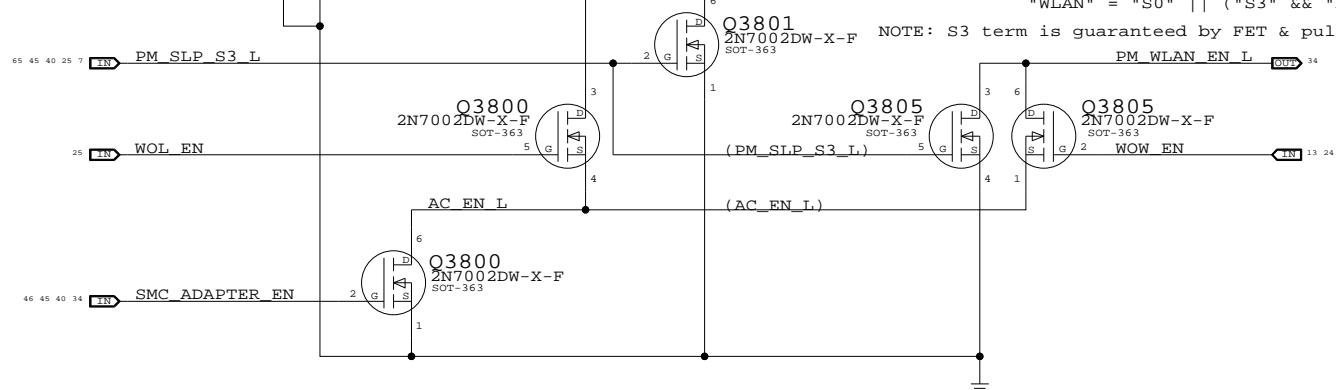
"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")
NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.



3.3V ENET FET

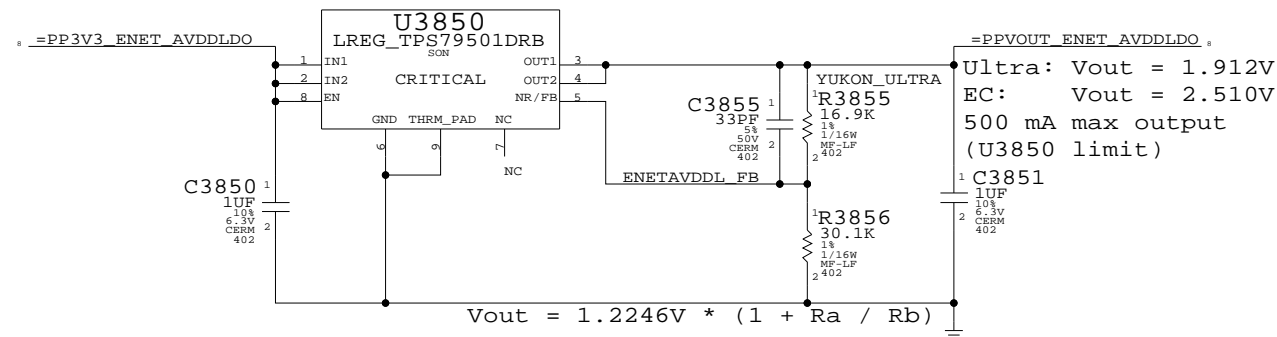
WLAN Enable Generation

"WLAN" = "S0" || ("S3" && "AC" && "WOW_EN")
NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.



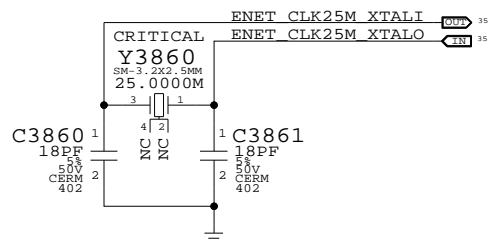
Yukon AVDDL LDO

1.9V for Yukon Ultra, 2.5V for Yukon EC
Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES,31.6K,1%,1/16W,402,LF	R3855		YUKON_EC

Yukon Crystal



Yukon Power Control

SYNC_MASTER=T9_NOME SYNC_DATE=03/16/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0
SCALE	SHT	OF
NONE	36	88

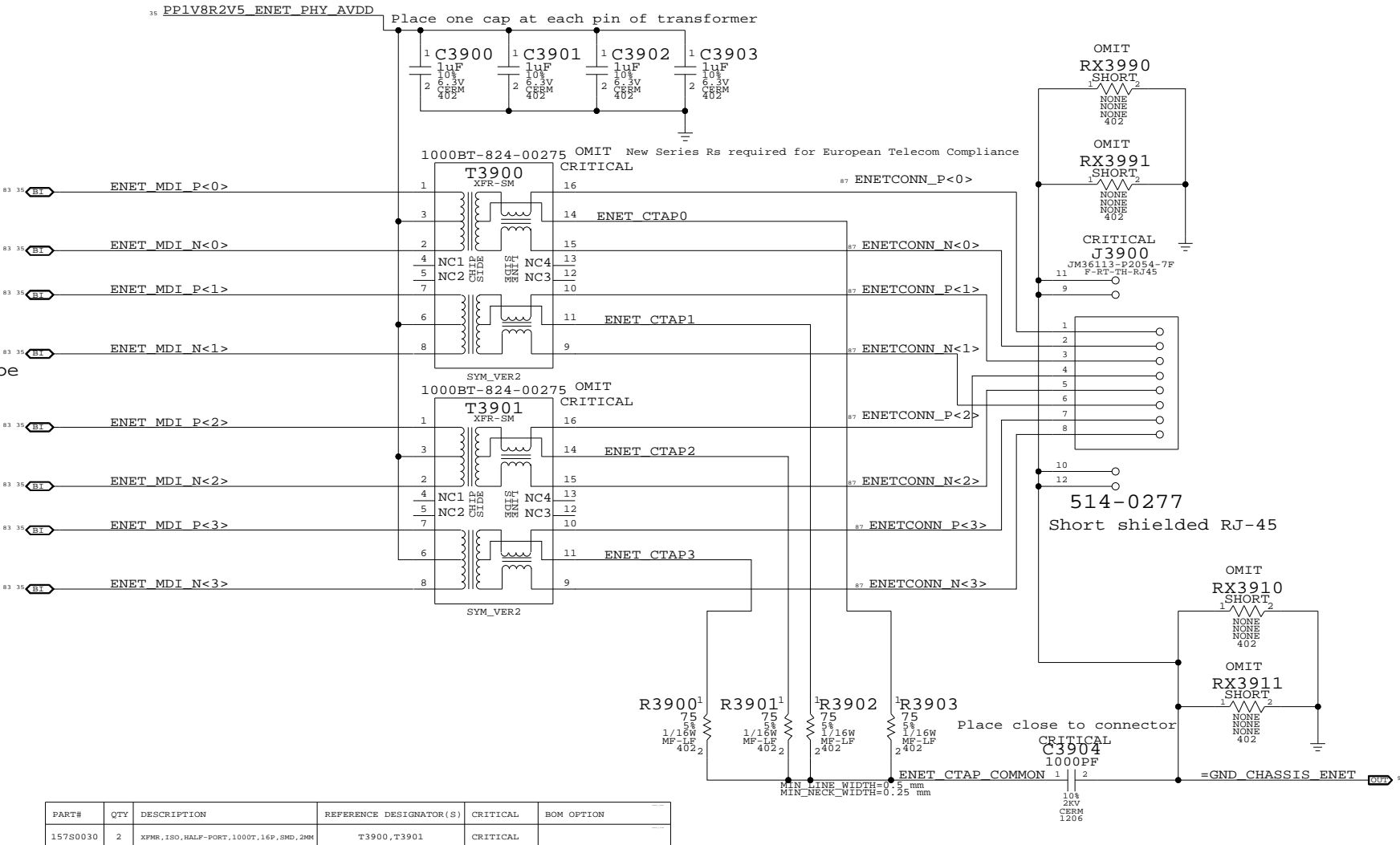
Page Notes

Power aliases required by this page:
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board



Ethernet Connector

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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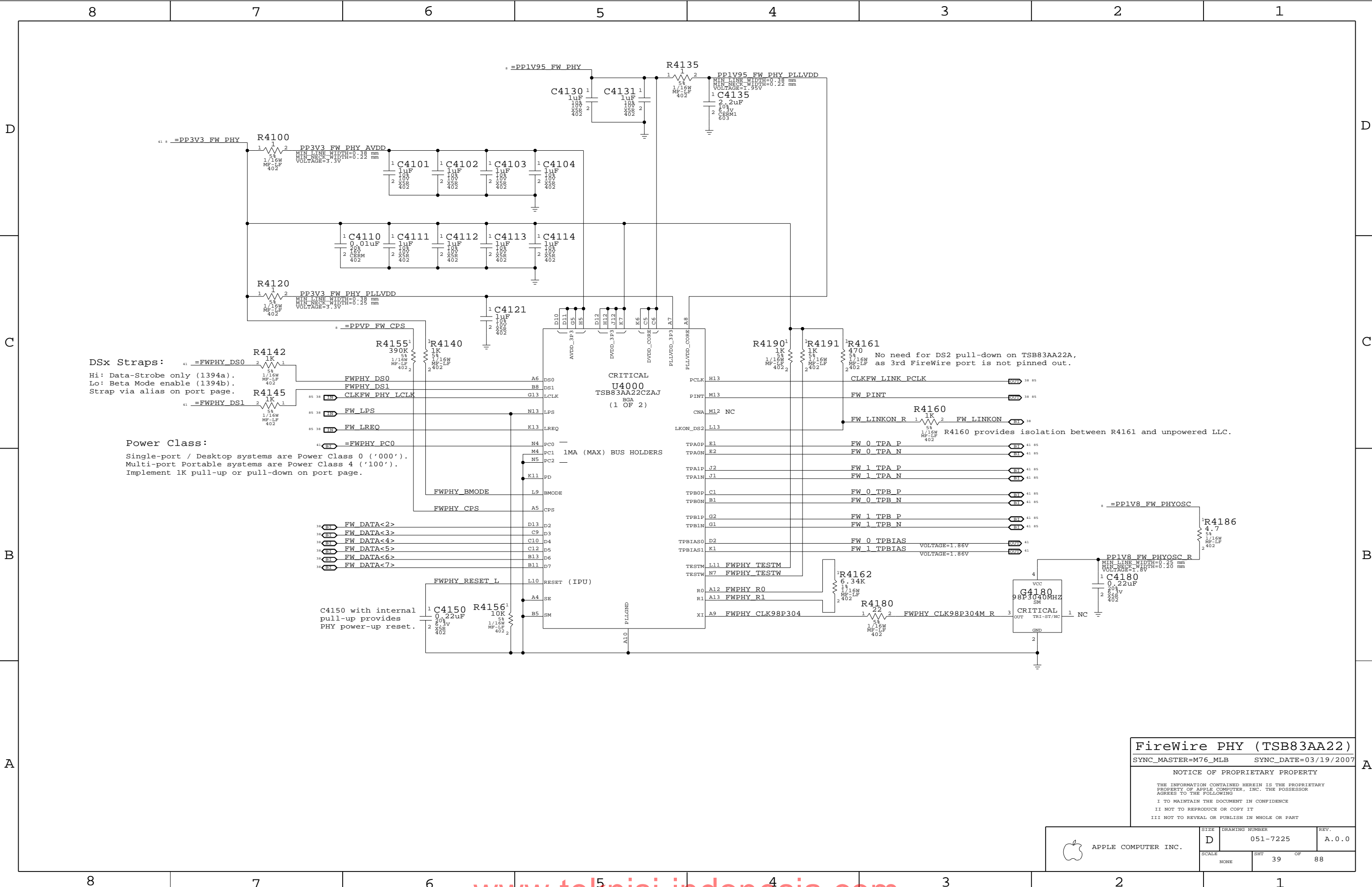
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0
SCALE	SHT	OF
NONE	37	88



FireWire PHY (TSB83AA22)

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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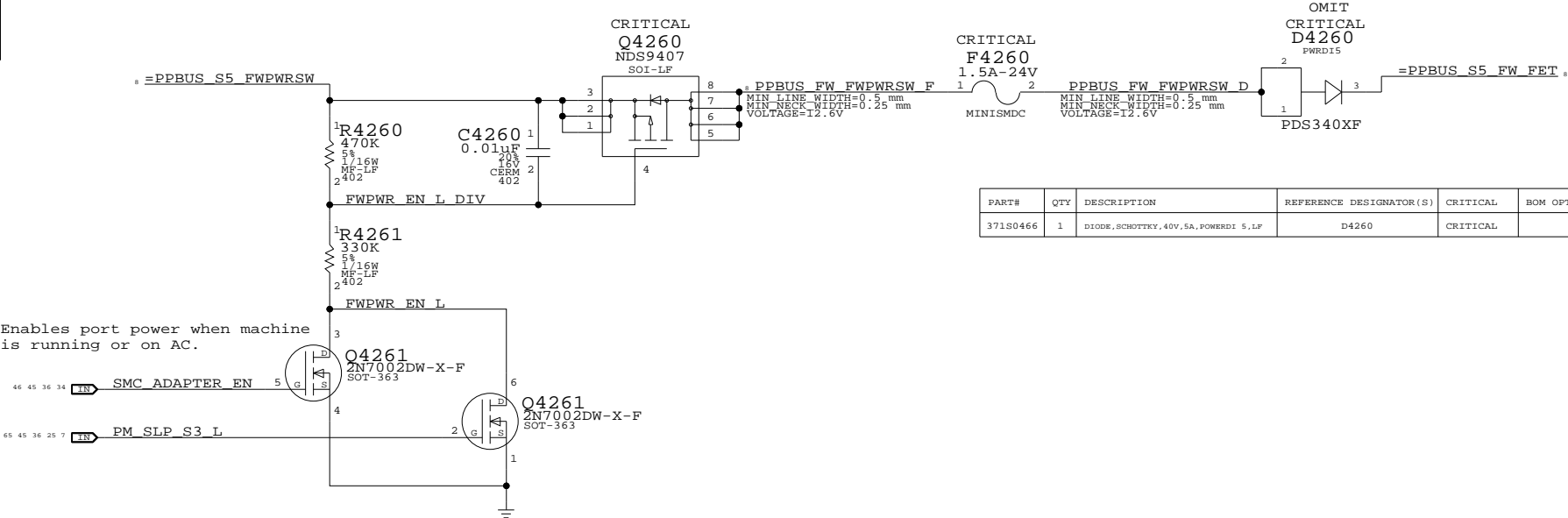
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	A.0.0
SCALE		SHT	OF
NONE		39	88

Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
- FW_PORT_FAULT_PU

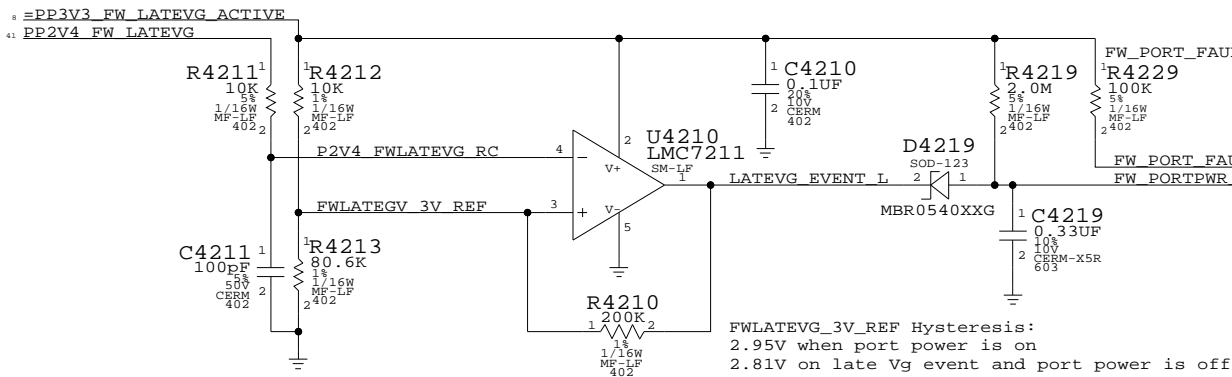
FireWire Port Power Switch



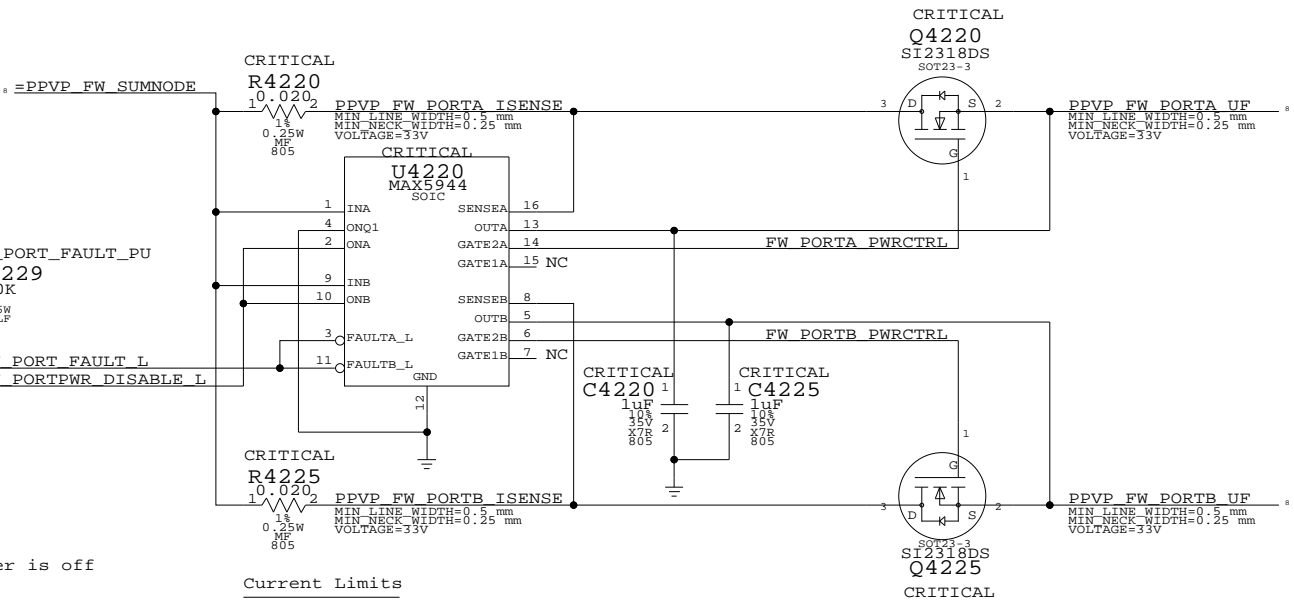
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
371S0466	1	DIODE,SCHOTTKY,40V,5A,POWERDI 5,LF	D4260	CRITICAL	

Current Limit/Active Late-VG Protection

Late-VG Event Detection



FWLATEVG_3V_REF Hysteresis:
2.95V when port power is on
2.81V on late Vg event and port power is off



Current Limits
0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0
SCALE	SHT	OF
NONE	40	88

8	7	6	5	4	3	2	1
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D

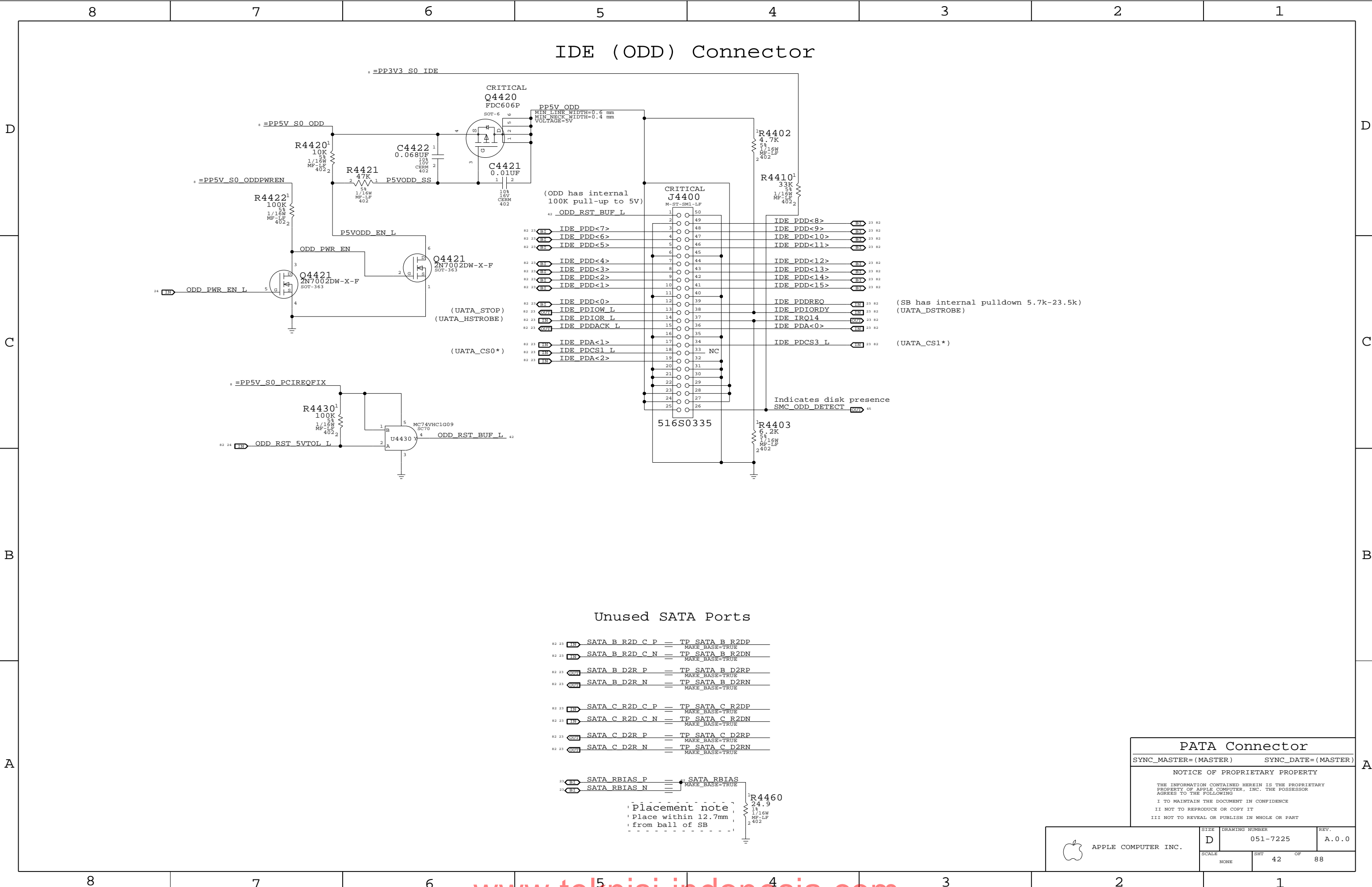
C

B

A

[illegible]

SIZE D	DRAWING NUMBER 051-7225	REV. A.0.0
SCALE NONE	SHT 41	OF 88



IDE (ODD) Connector

Unused SATA Ports

82 23	TP	SATA B R2D C P	==	TP SATA B R2DP	MAKE_BASE=TRUE
82 23	TP	SATA B R2D C N	==	TP SATA B R2DN	MAKE_BASE=TRUE
82 23	TP	SATA B D2R P	==	TP SATA B D2RP	MAKE_BASE=TRUE
82 23	TP	SATA B D2R N	==	TP SATA B D2RN	MAKE_BASE=TRUE
82 23	TP	SATA C R2D C P	==	TP SATA C R2DP	MAKE_BASE=TRUE
82 23	TP	SATA C R2D C N	==	TP SATA C R2DN	MAKE_BASE=TRUE
82 23	TP	SATA C D2R P	==	TP SATA C D2RP	MAKE_BASE=TRUE
82 23	TP	SATA C D2R N	==	TP SATA C D2RN	MAKE_BASE=TRUE

23	TP	SATA RBIAS P	==	SATA RBIAS	MAKE_BASE=TRUE
23	TP	SATA RBIAS N	==	SATA RBIAS	MAKE_BASE=TRUE

Placement note
Place within 12.7mm
from ball of SB

PATA Connector

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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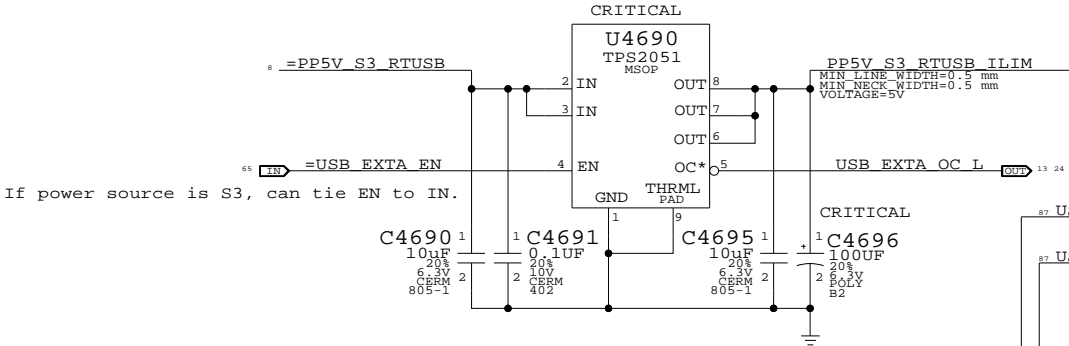
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART



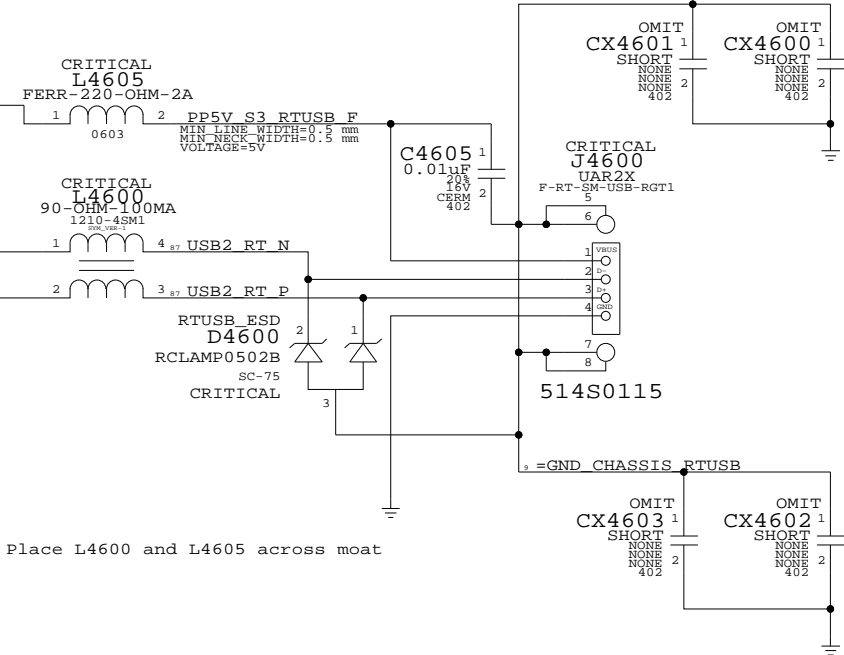
APPLE COMPUTER INC.

SIZE	D	DRAWING NUMBER	051-7225	REV.	A.0.0
SCALE	NONE	SHT	42	OF	88

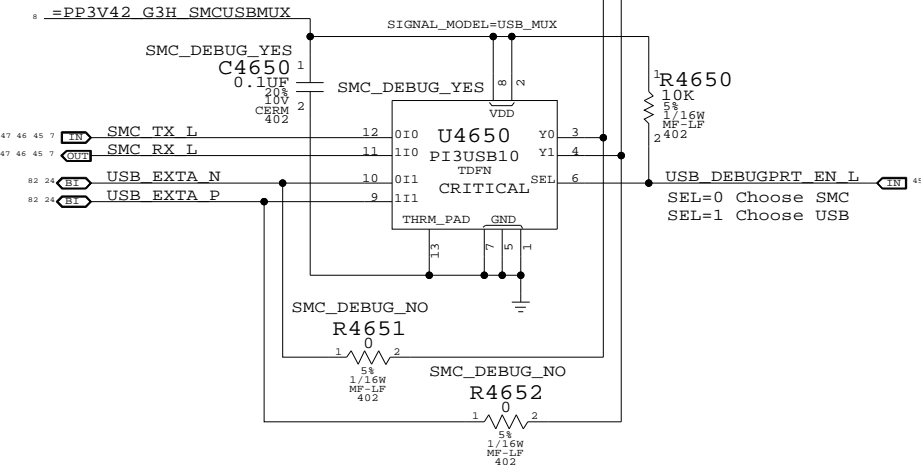
Port Power Switch



Right USB Port



USB/SMC Debug Mux



External USB Connector

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7225	REV. A.0.0
	SCALE NONE	SHT 43	OF 88

CRITICAL
L4730
FERR-220-OHM-2A =PP5V S3 CAMERA 7 8

PP5V S3 CAMERA F
MIN LINE WIDTH=0.25 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=5V
NO STUFF
C4730 0.001uF
0.001uF
50V 278 402

CRITICAL
FL4735
90-OHM-100MA
1210-4SM1
100-10-1

CRITICAL
L4731
FERR-220-OHM-2A

OMIT
CRITICAL
L4731
FERR-220-OHM-2A

Keep close to FL4735 to keep return current loop small

CRITICAL
L4740
FERR-220-OHM-2A =PP5V S3 WWAN 7 8

PP5V S3 WWAN F
MIN LINE WIDTH=0.25 mm
MIN NECK WIDTH=0.2 mm
VOLTAGE=5V
NOSTUFF
C4741 0.001uF
0.001uF
50V 278 402

CRITICAL
FL4745
90-OHM-100MA
1210-4SM1
100-10-1

CRITICAL
L4741
FERR-220-OHM-2A

OMIT
CRITICAL
L4741
FERR-220-OHM-2A

Keep close to FL4745 to keep return current loop small

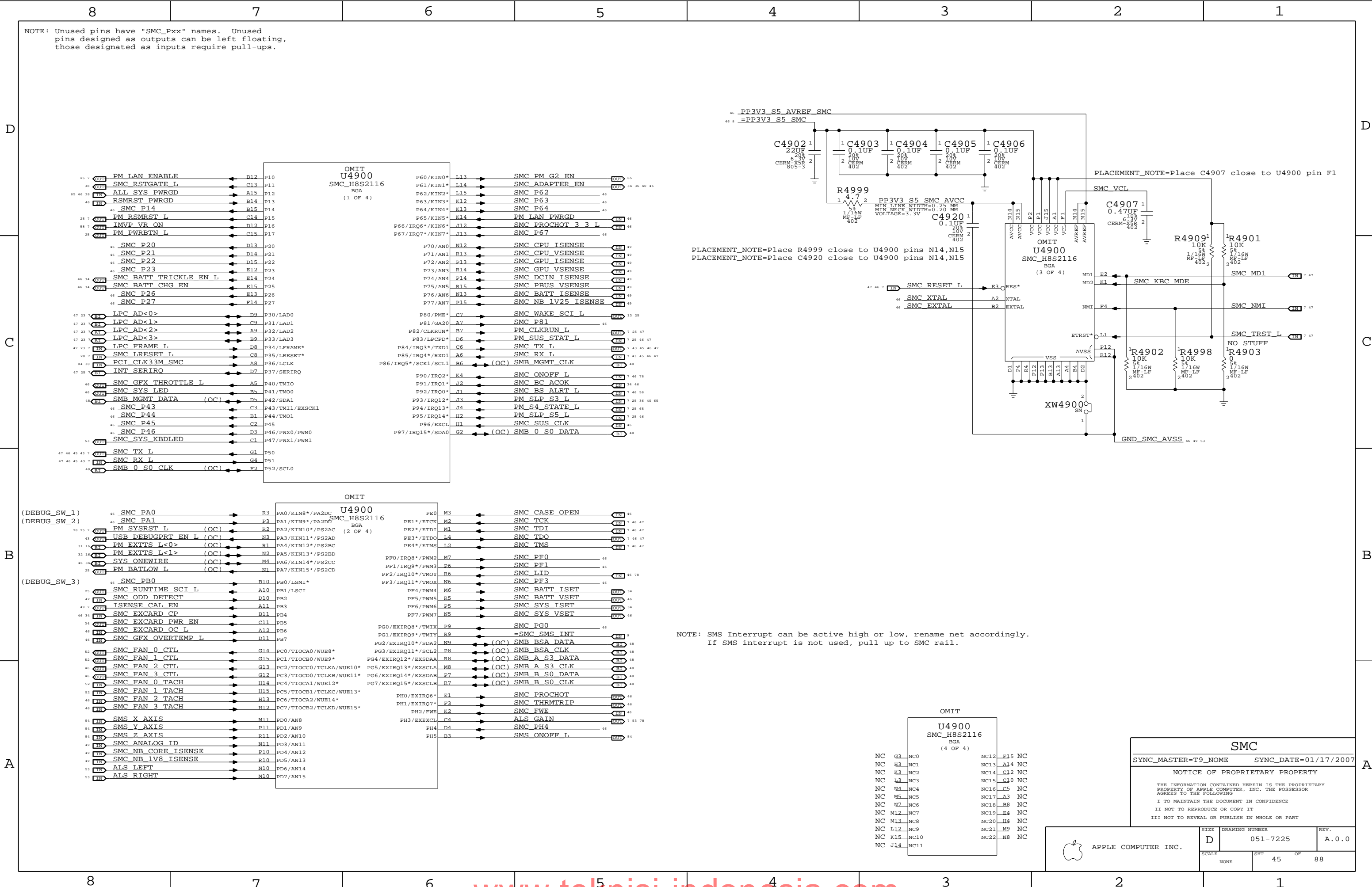
514S0171

_GND_CHASSIS_LEFTCLUTCH

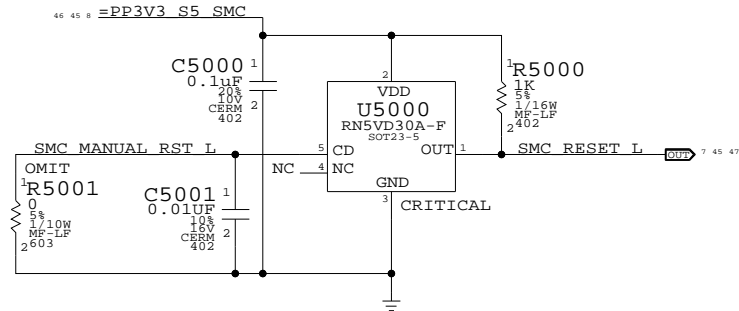
SIM Interconnect

Left Clutch Barrel Interconnect	
SYNC_MASTER=M76_MLB	SYNC_DATE=03/19/2007
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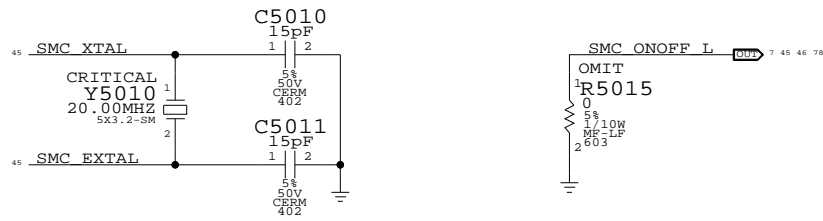
www.teknisi-indonesia.com



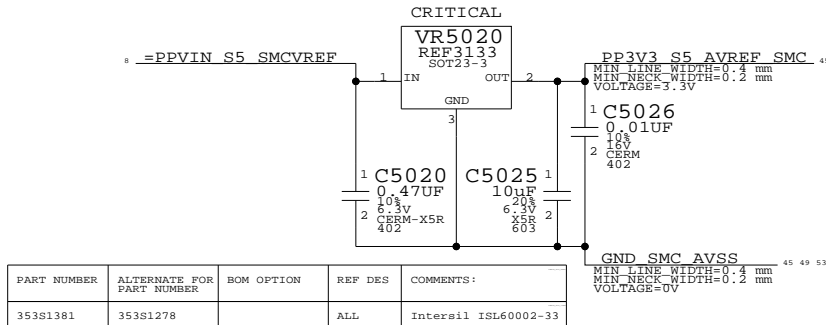
SMC Reset "Button" / Brownout Detect



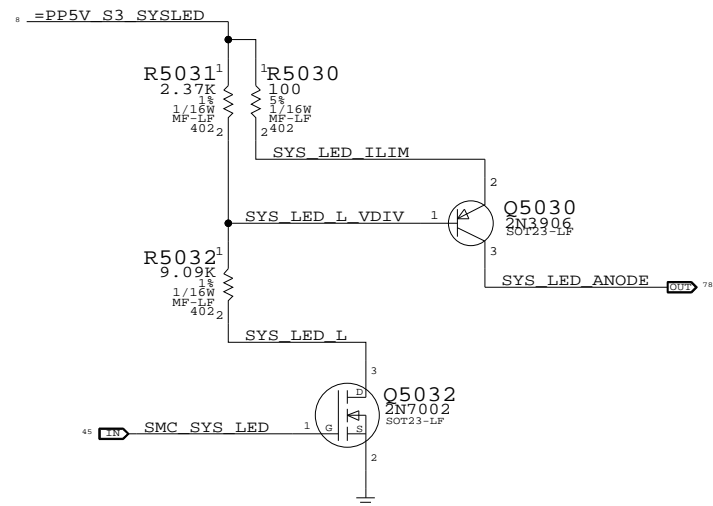
SMC Crystal Circuit Debug Power "Button"



SMC AVREF Supply



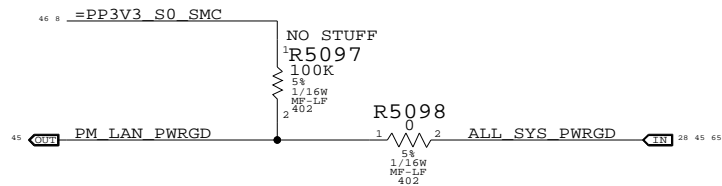
System (Sleep) LED Circuit



SMC FAN 2 CTL	=	TP_SMC_FAN_2_CTL
SMC FAN 2 TACH	=	TP_SMC_FAN_2_TACH
SMC FAN 3 CTL	=	TP_SMC_FAN_3_CTL
SMC FAN 3 TACH	=	TP_SMC_FAN_3_TACH
SMC GFX OVERTEMP L	=	TP_SMC_GFX_OVERTEMP_L
SMC GFX THROTTLE L	=	TP_SMC_GFX_THROTTLE_L
SMC BATT VSET	=	TP_SMC_BATT_VSET
SMC SYS VSET	=	TP_SMC_SYS_VSET
SMC P14	=	TP_SMC_P14
SMC P20	=	TP_SMC_P20
SMC P21	=	TP_SMC_P21
SMC P22	=	TP_SMC_P22
SMC P23	=	TP_SMC_P23
SMC P26	=	TP_SMC_P26
SMC P27	=	TP_SMC_P27
SMC P43	=	TP_SMC_P43
SMC P44	=	TP_SMC_P44
SMC P46	=	TP_SMC_P46
SMC P62	=	TP_SMC_P62
SMC P63	=	TP_SMC_P63
SMC P64	=	TP_SMC_P64
SMC P81	=	TP_SMC_P81
SMC PF0	=	TP_SMC_PF0
SMC PF1	=	TP_SMC_PF1

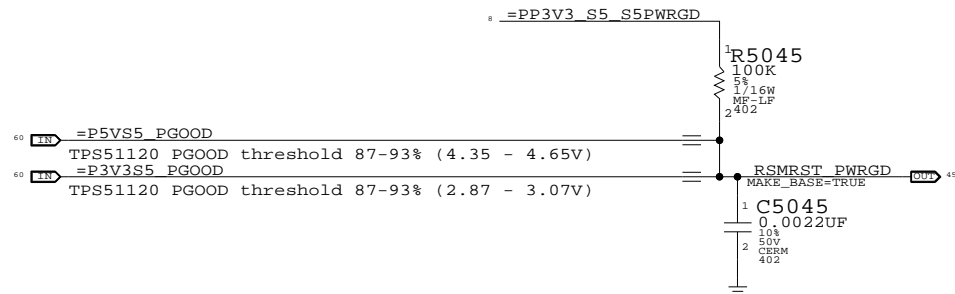
SMC EXCARD_OC_L	=	EXCARD_OC_L
SMC_SUS_CLK	=	SUS_CLK_SB
SMC_P45	=	SMC_ENRGYSTRLDO_EN

LAN PWRGD Circuit

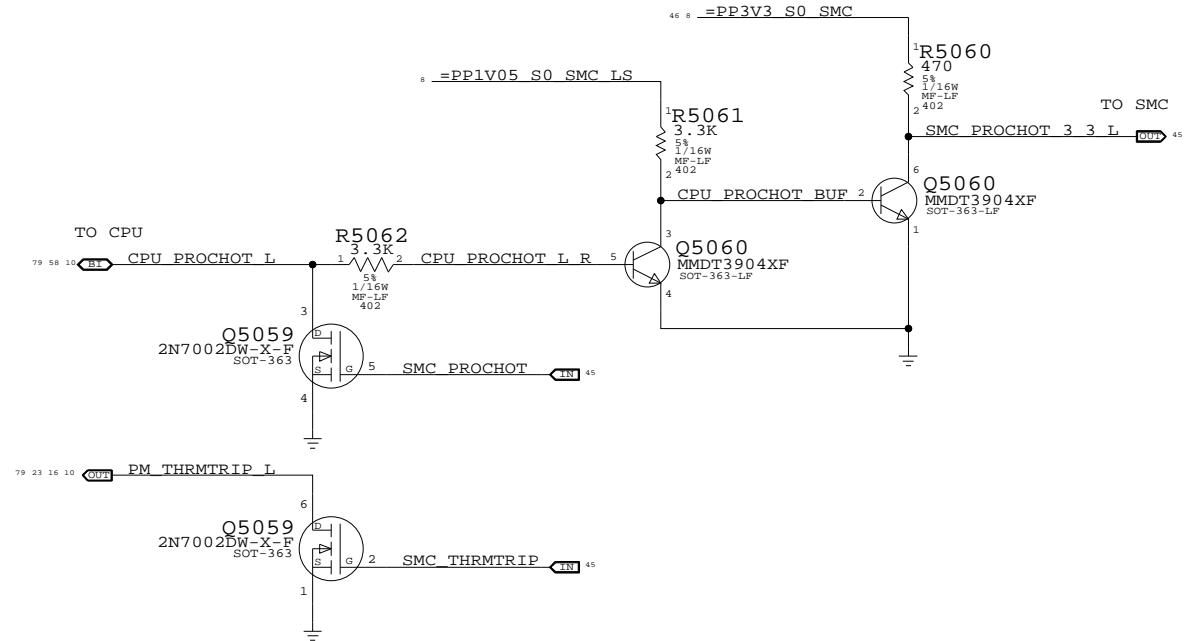


S5 Rail PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation



SMC FSB to 3.3V Level Shifting



SMC_PA0	R5091	100K	5% 1/16W MF-LF 402
SMC_PA1	R5092	100K	5% 1/16W MF-LF 402
SMC_PB0	R5093	100K	5% 1/16W MF-LF 402
SMC_ONOFF_L	R5070	10K	5% 1/16W MF-LF 402
SMC_LID	R5071	100K	5% 1/16W MF-LF 402
SMC_FWE	R5072	10K	5% 1/16W MF-LF 402
SMC_TX_L	R5073	10K	5% 1/16W MF-LF 402
SMC_RX_L	R5074	100K	5% 1/16W MF-LF 402
SYS_ONEWIRE	R5075	2.0K	5% 1/16W MF-LF 402
SMC_BS_ALRT_L	R5076	100K	5% 1/16W MF-LF 402
SMC_TMS	R5077	10K	5% 1/16W MF-LF 402
SMC_TDO	R5078	10K	5% 1/16W MF-LF 402
SMC_TDI	R5079	10K	5% 1/16W MF-LF 402
SMC_TCK	R5080	10K	5% 1/16W MF-LF 402
SMC_P67	R5094	10K	5% 1/16W MF-LF 402
SMC_PF3	R5081	10K	5% 1/16W MF-LF 402
SMC_PG0	R5096	10K	5% 1/16W MF-LF 402
SMC_PH4	R5082	10K	5% 1/16W MF-LF 402
SMC_BATT_TRICKLE_EN_L	R5083	10K	5% 1/16W MF-LF 402
SMC_BATT_CHG_EN	R5084	10K	5% 1/16W MF-LF 402
SMC_ADAPTER_EN	R5085	10K	5% 1/16W MF-LF 402
SMC_CASE_OPEN	R5086	10K	5% 1/16W MF-LF 402
SMC_BC_ACOK	R5087	470K	5% 1/16W MF-LF 402
SMC_EXCARD_CP	R5088	10K	5% 1/16W MF-LF 402
PM_SUS_STAT_L	R5089	100K	5% 1/16W MF-LF 402
PM_SLP_S5_L	R5090	100K	5% 1/16W MF-LF 402

SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

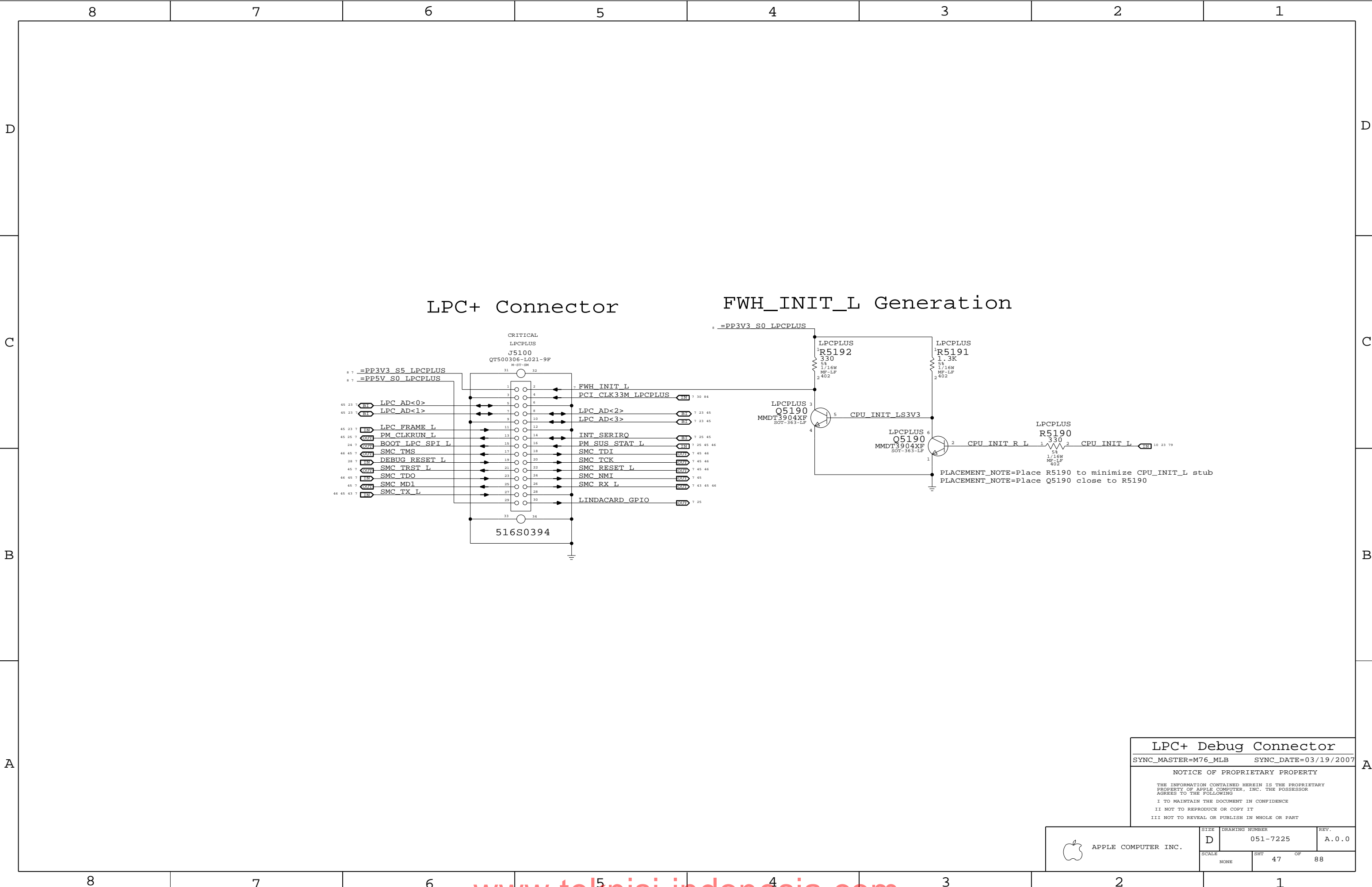
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SCALE	NONE	SHT	46	OF	88



LPC+ Debug Connector

SYNC_MASTER=M76_MLB

SYNC_DATE=03/19/2007

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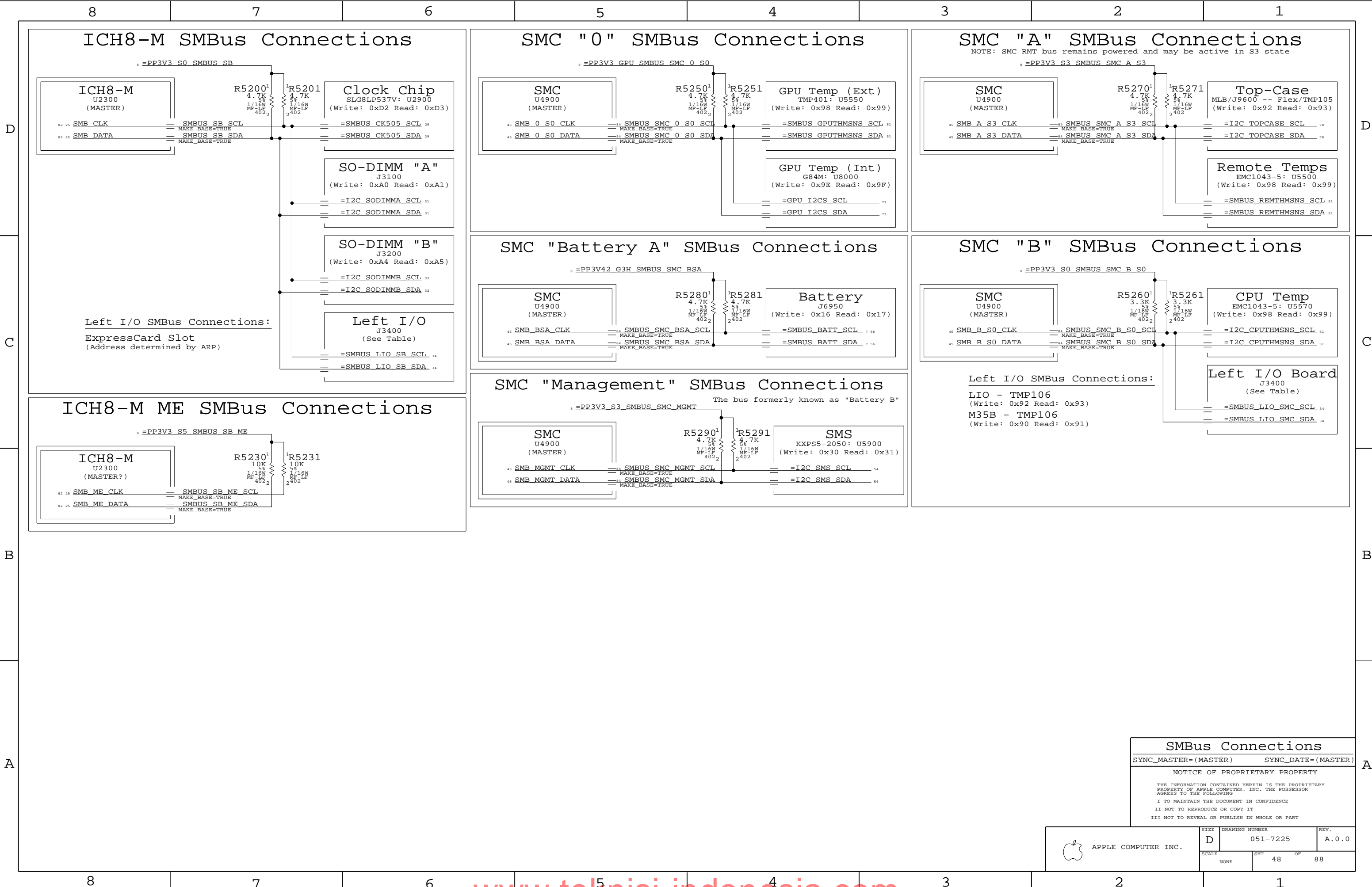
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SCALE		SHT	OF
NONE		47	88



SMBus Connections

SYNC_MASTER= (MASTER)

SYNC_DATE= (MASTER)


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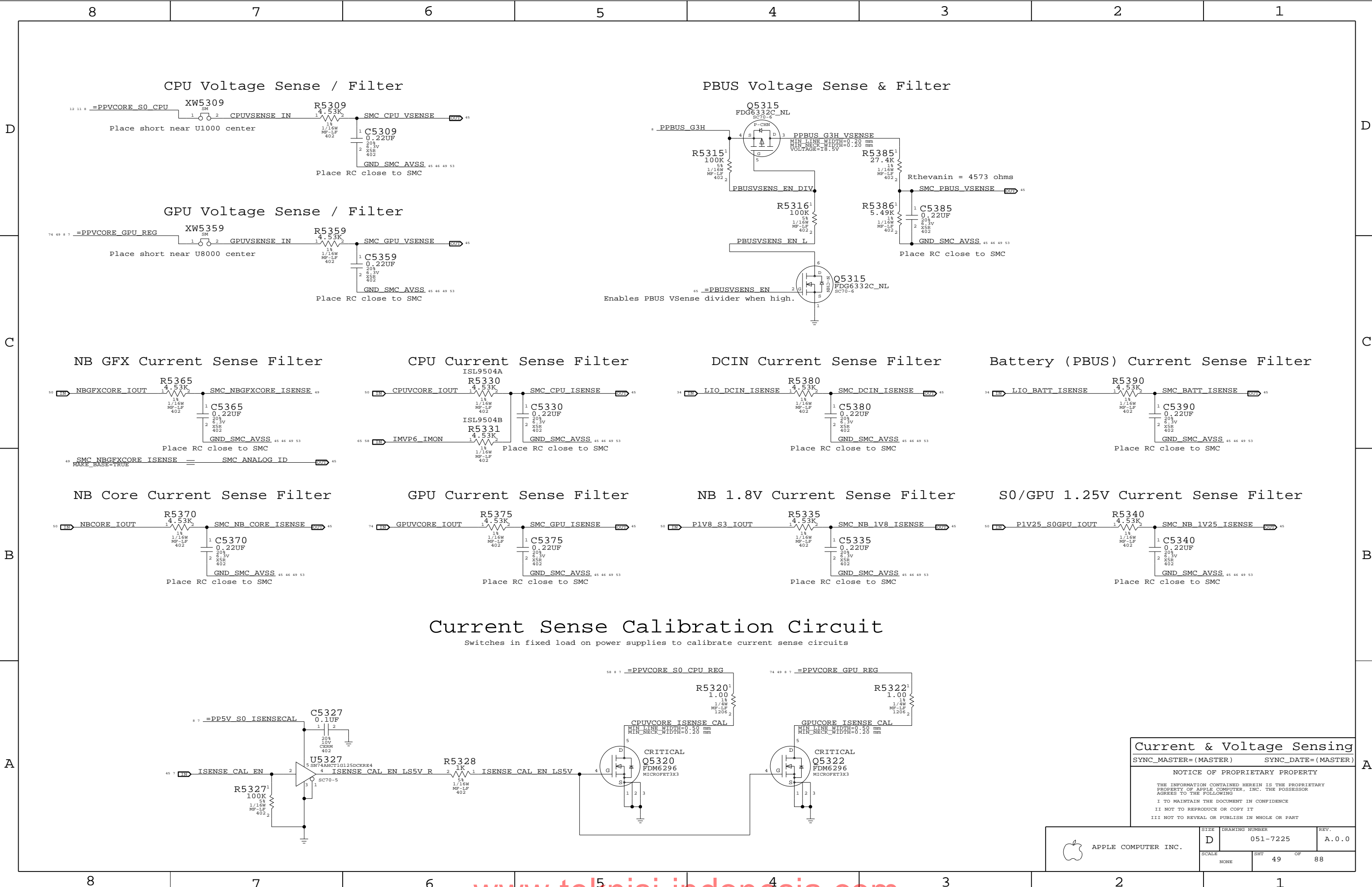
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	NONE	48	88	



CPU Voltage Sense / Filter

PBUS Voltage Sense & Filter

GPU Voltage Sense / Filter

NB GFX Current Sense Filter

CPU Current Sense Filter

DCIN Current Sense Filter

Battery (PBUS) Current Sense Filter

NB Core Current Sense Filter

GPU Current Sense Filter

NB 1.8V Current Sense Filter

S0/GPU 1.25V Current Sense Filter

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits

Current & Voltage Sensing

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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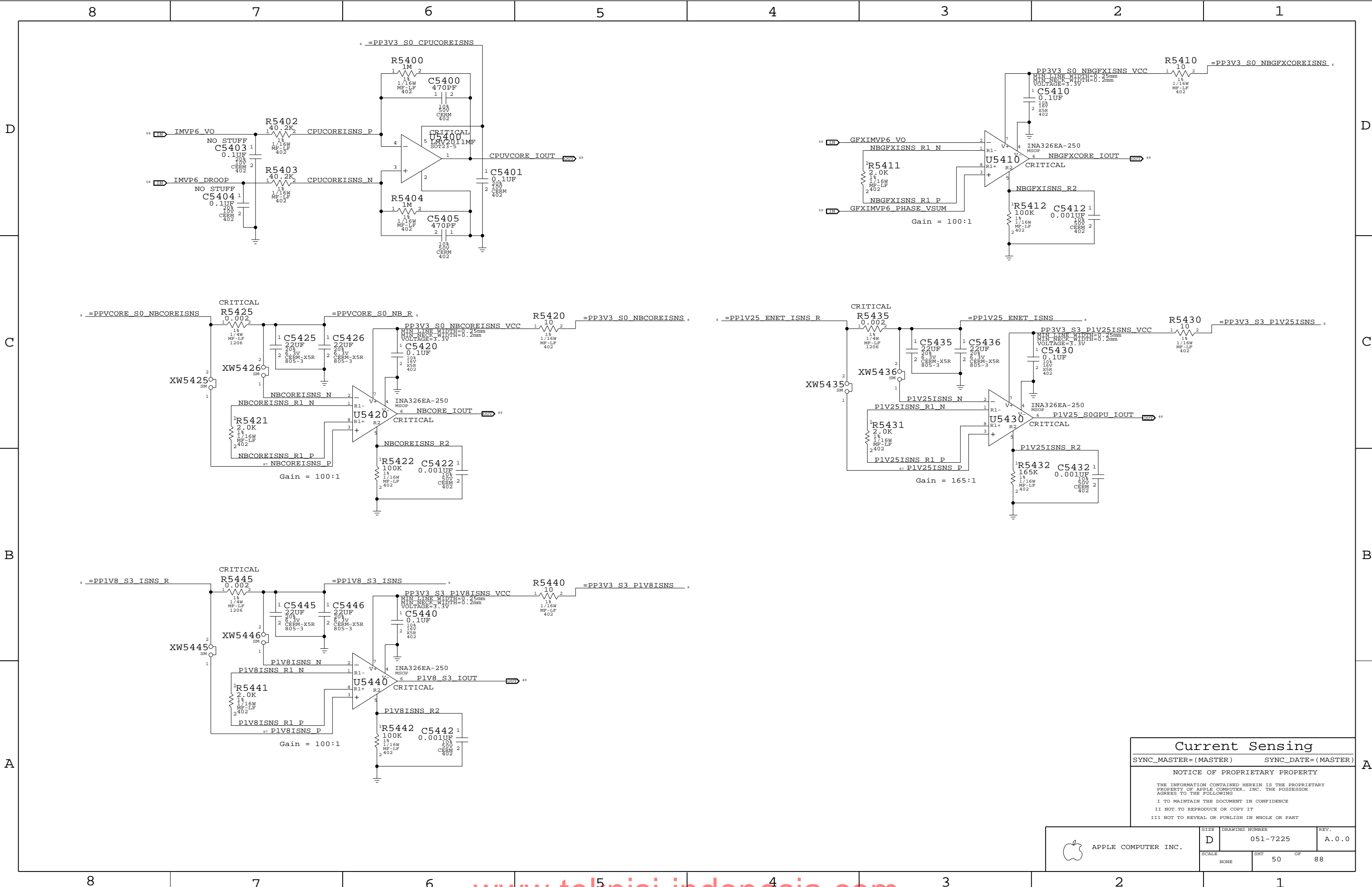
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SCALE	NONE	SHT	49	OF	88



Current Sensing

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

NOTICE OF PROPRIETARY PROPERTY

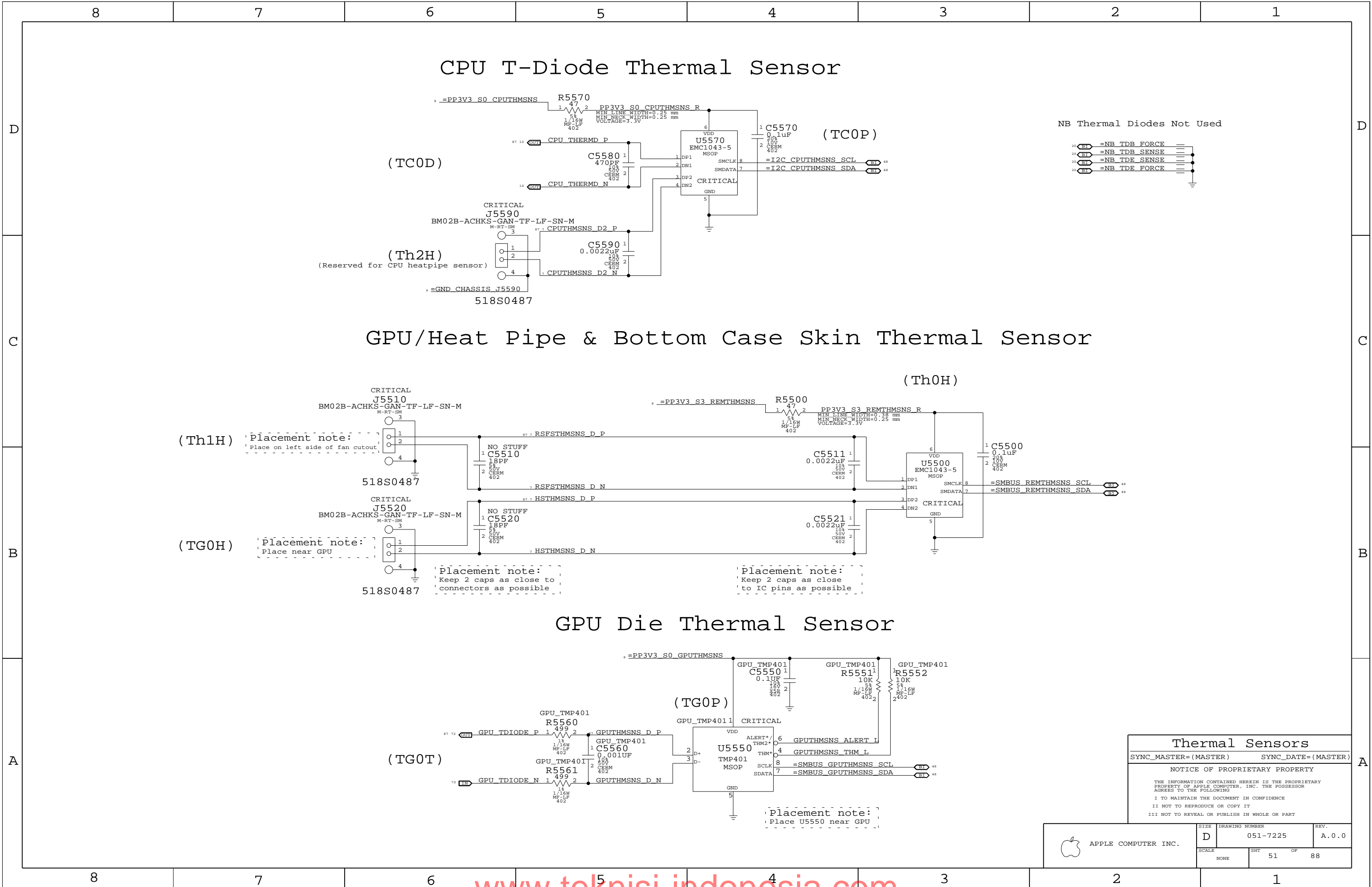
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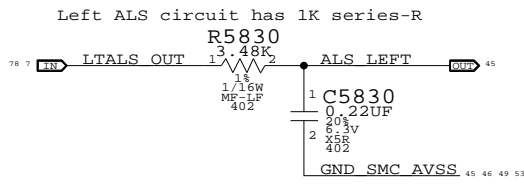
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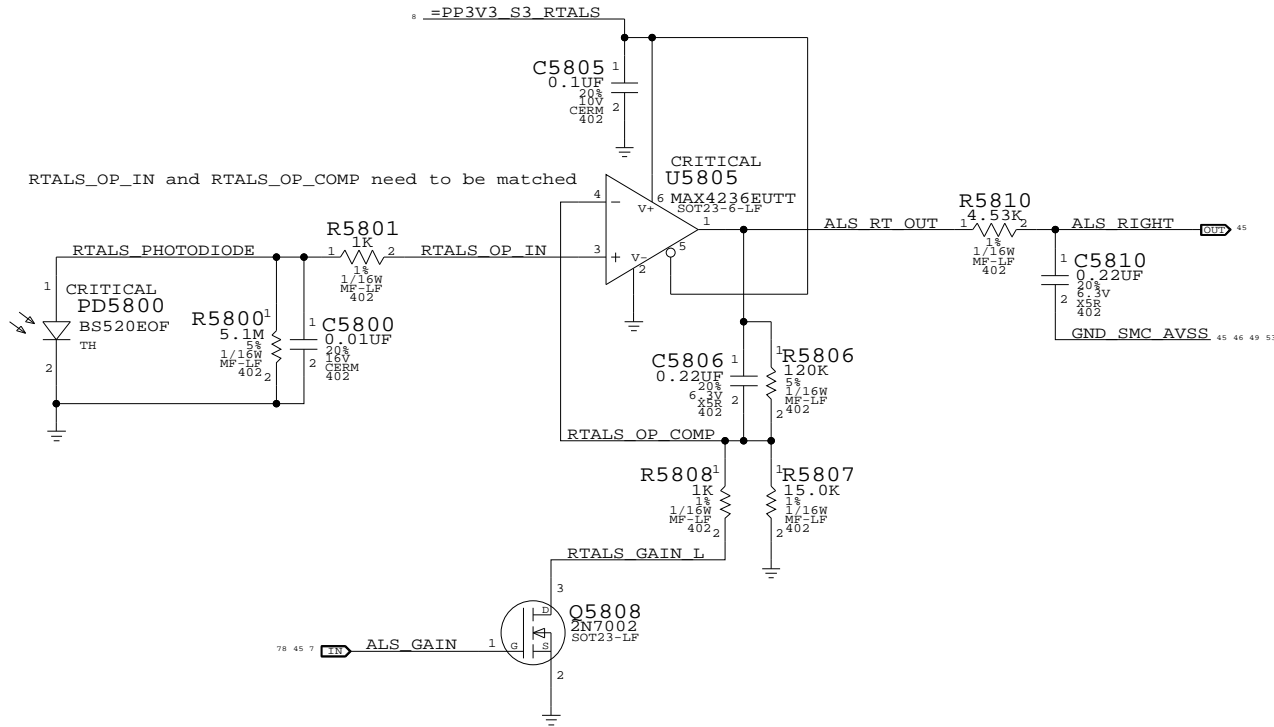
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SCALE		SHT	OF
NONE		50	88



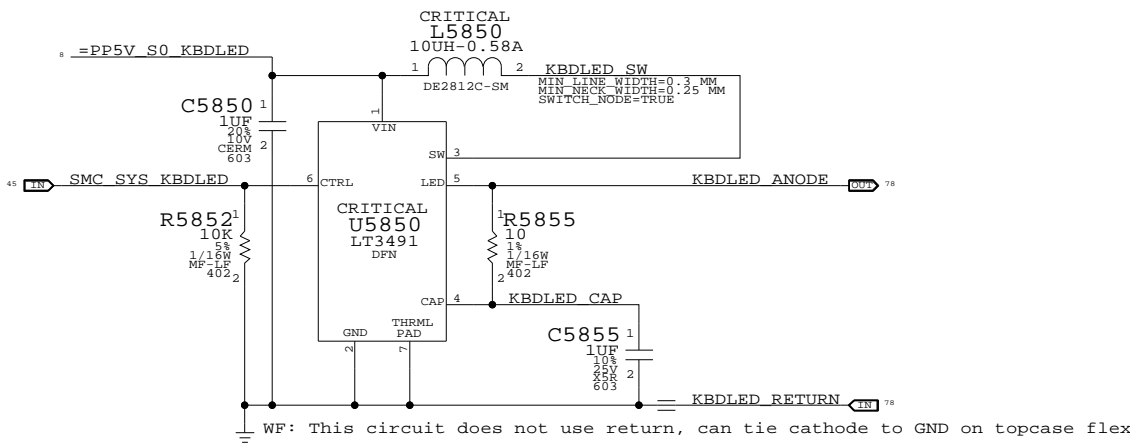
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



ALS Support

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

NOTICE OF PROPRIETARY PROPERTY

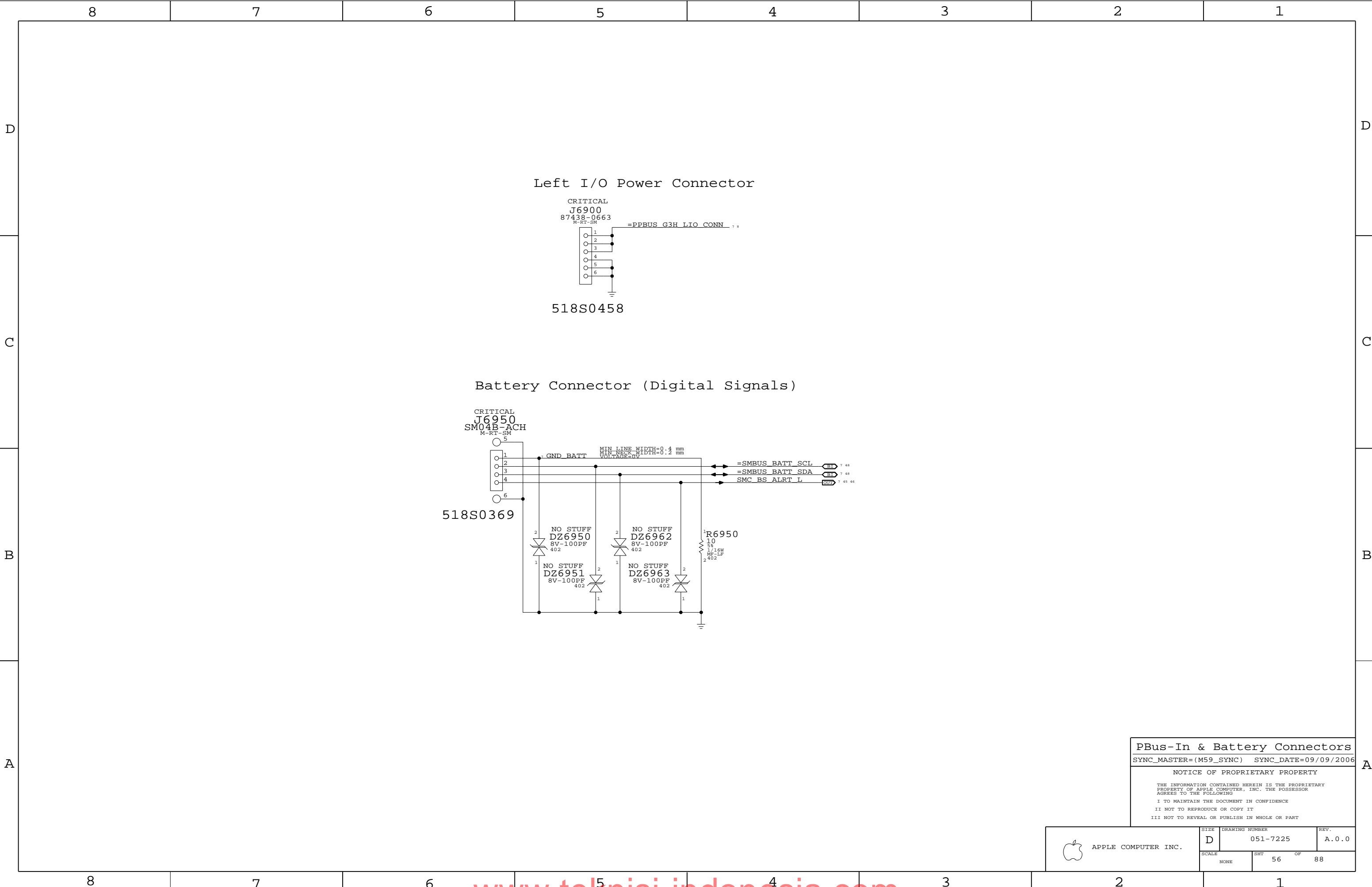
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SCALE		SHT	OF
NONE		53	88



PBus-In & Battery Connectors

SYNC_MASTER=(M59_SYNC) SYNC_DATE=09/09/2006

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APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7225

REV.

A.0.0

SCALE

NONE

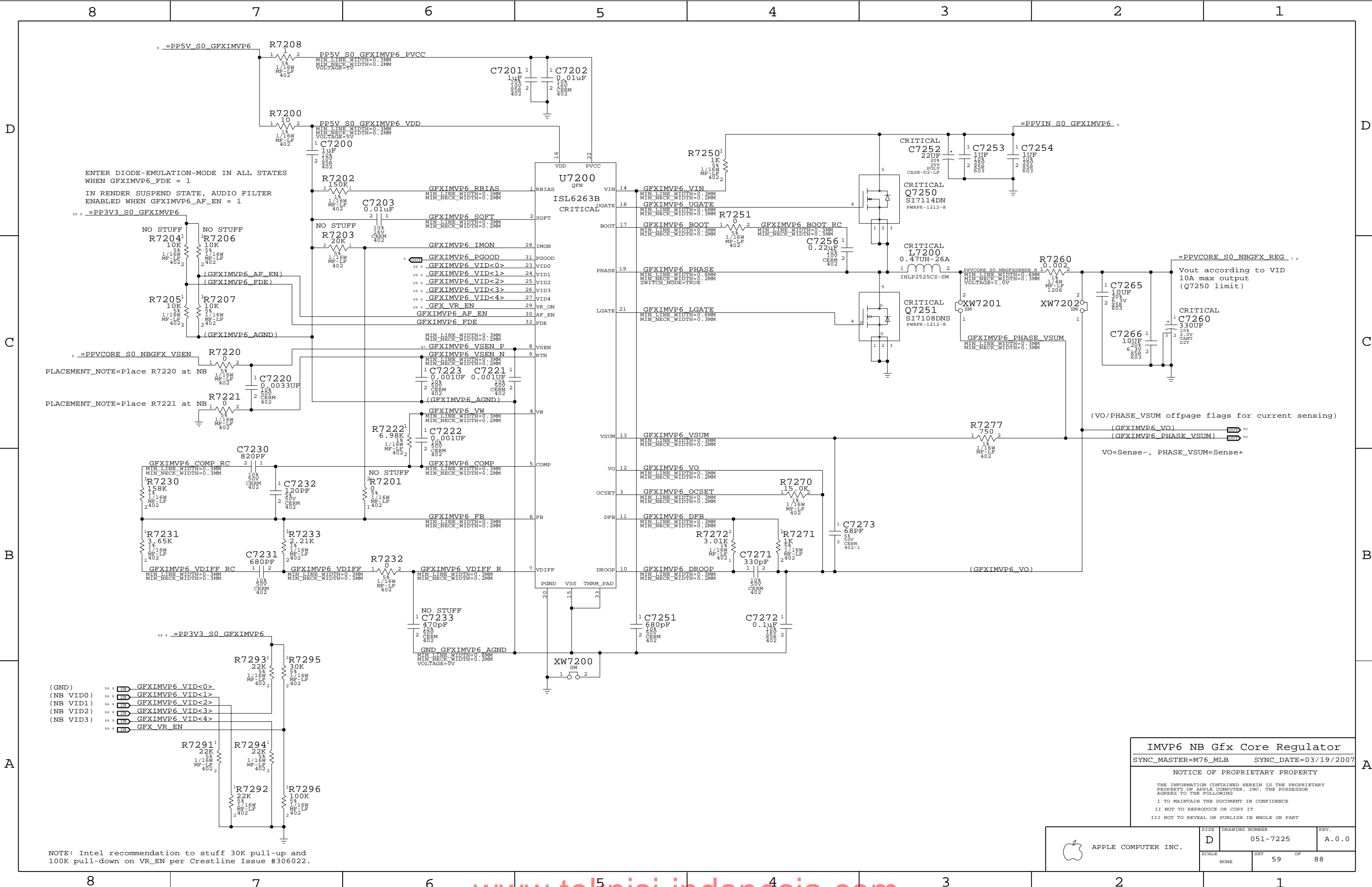
SHT

56

OF

88





IMVP6 NB Gfx Core Regulator

SYNC_MASTER=M76_MLB

SYNC_DATE=03/19/2007


NOTICE OF PROPRIETARY PROPERTY

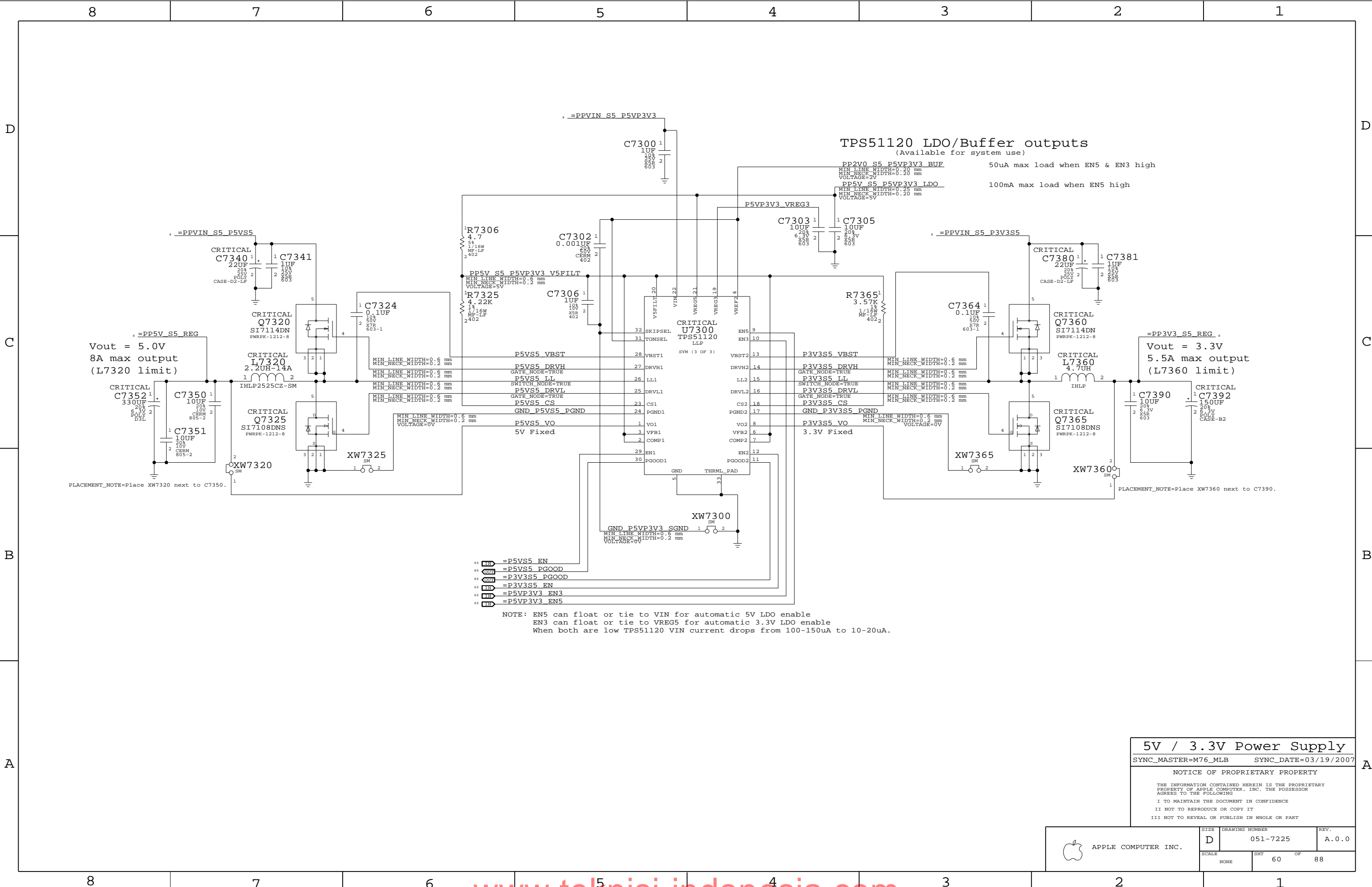
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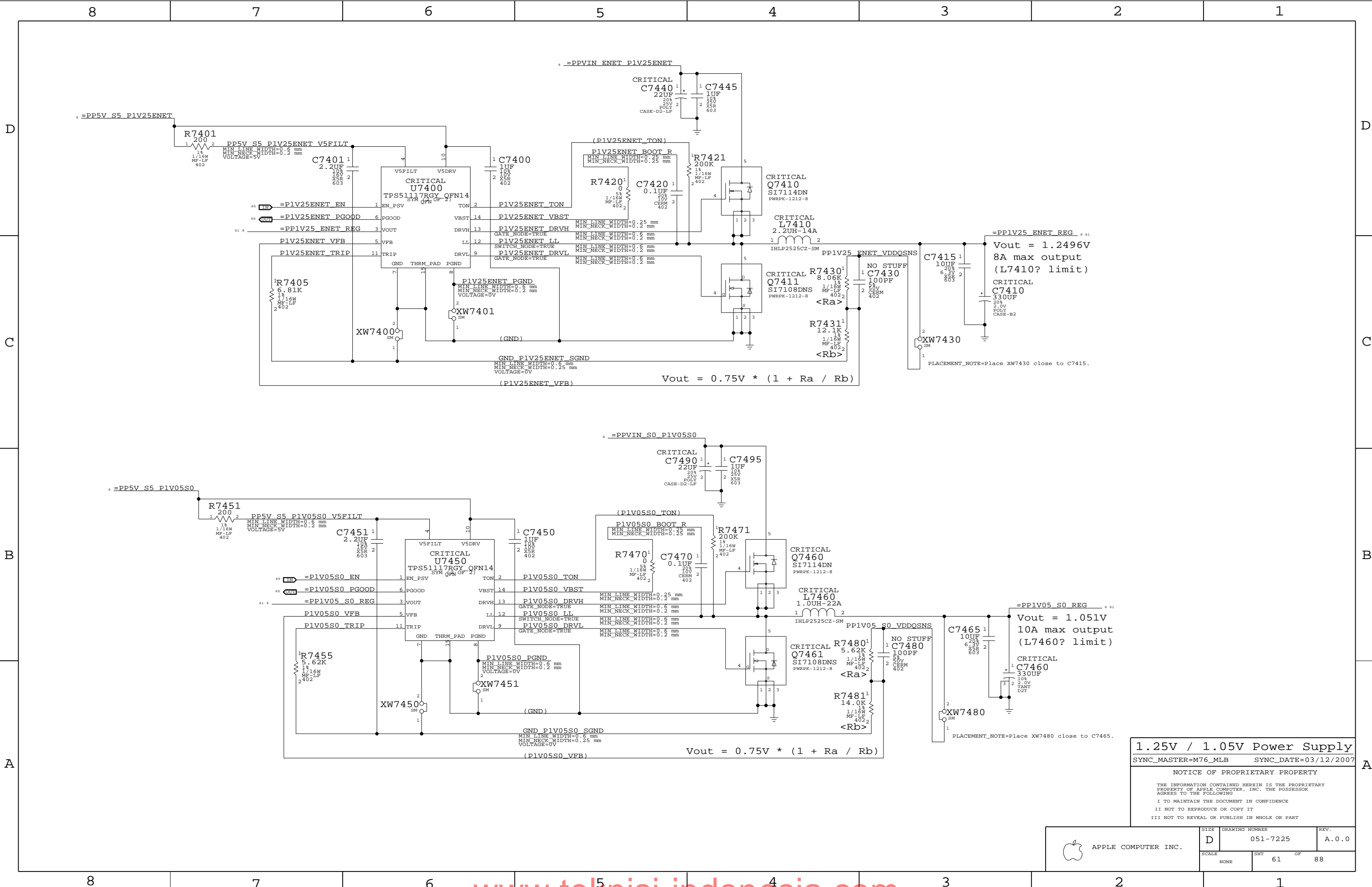
 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER		REV.
	D	051-7225		A.0.0
	SCALE NONE	SHT 59	OF 88	



NOTE: EN5 can float or tie to VIN for automatic 5V LDO enable
EN3 can float or tie to VREG5 for automatic 3.3V LDO enable
When both are low TPS51120 VIN current drops from 100-150uA to 10-20uA.

5V / 3.3V Power Supply
SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007
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	D	051-7225	A.0.0
SCALE		SHT	OF
NONE		60	88



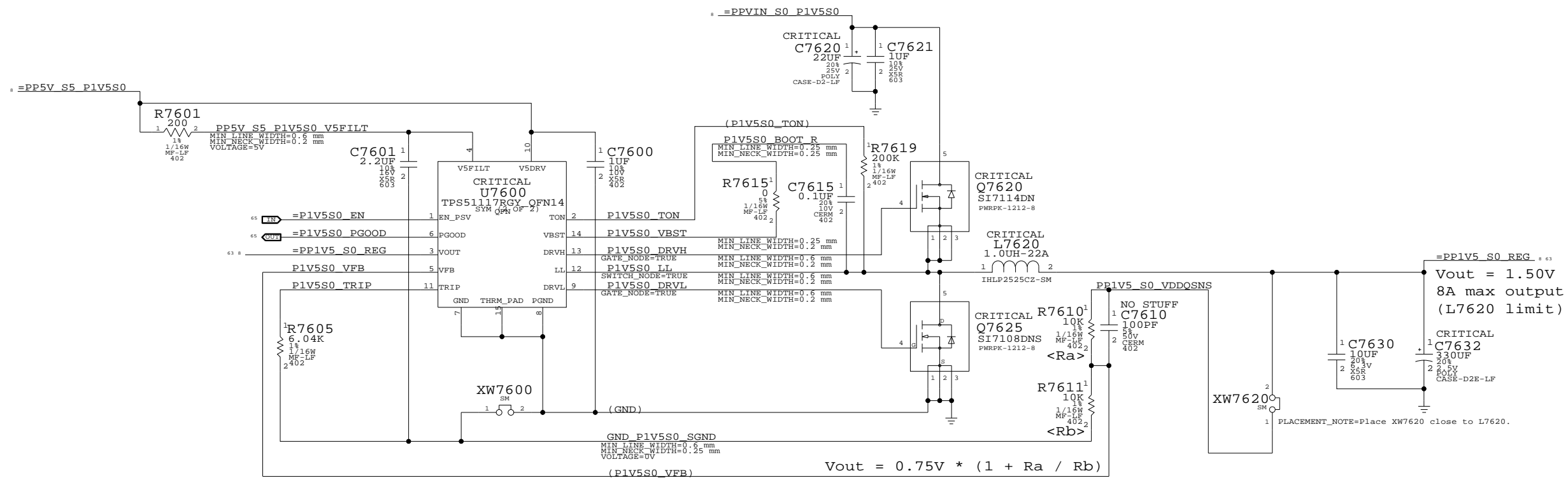
1.25V / 1.05V Power Supply

SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007

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	SCALE NONE	SHT 61	OF 88



1.5V Power Supply
SYNC_MASTER=M76_MLB SYNC_DATE=03/12/2007
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	SCALE NONE	SHT 63	OF 88

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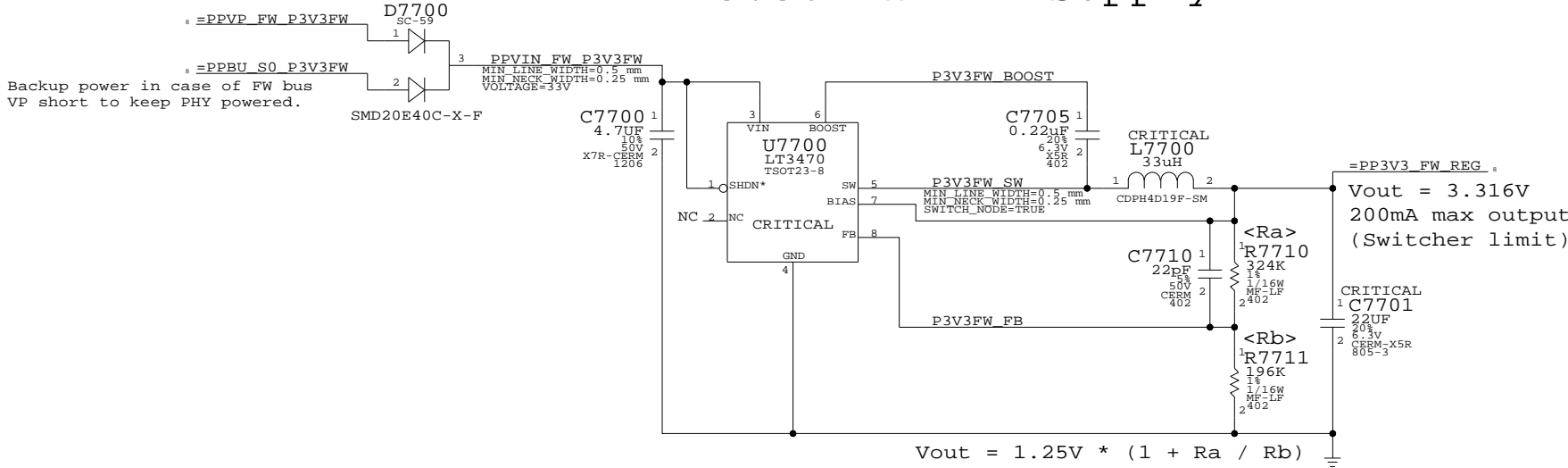
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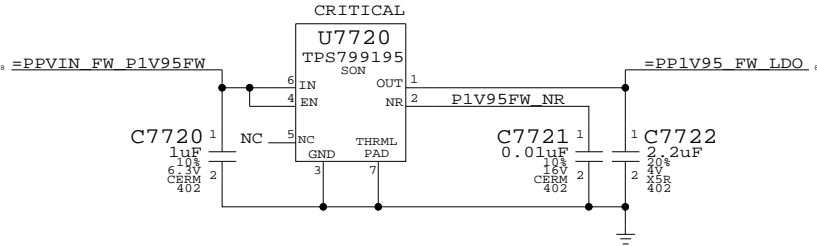
B

A

3.3V FW PHY Supply



1.95V FW PHY Supply



FW PHY Power Supplies

SYNC_MASTER=M76_MLB SYNC_DATE=03/19/2007

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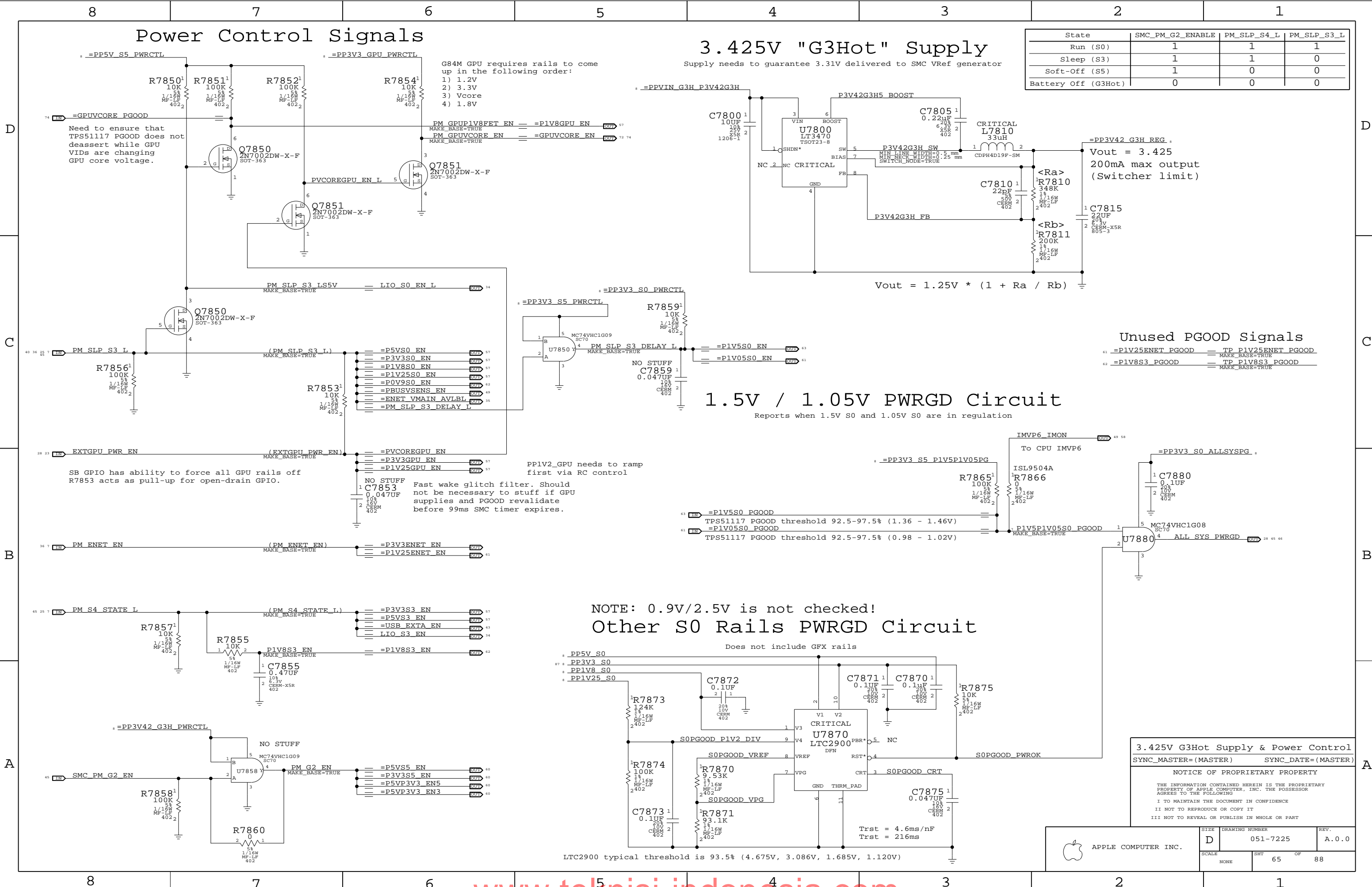
NONE

SHT

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OF

88



Power Control Signals

3.425V "G3Hot" Supply

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

Vout = 3.425
200mA max output
(Switcher limit)

$$V_{out} = 1.25V * (1 + R_a / R_b)$$

Unused PG00D Signals

=P1V25ENET PG00D	=TP P1V25ENET PG00D
=P1V8S3 PG00D	=TP P1V8S3 PG00D

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

NOTE: 0.9V/2.5V is not checked!
Other S0 Rails PWRGD Circuit

3.425V G3Hot Supply & Power Control

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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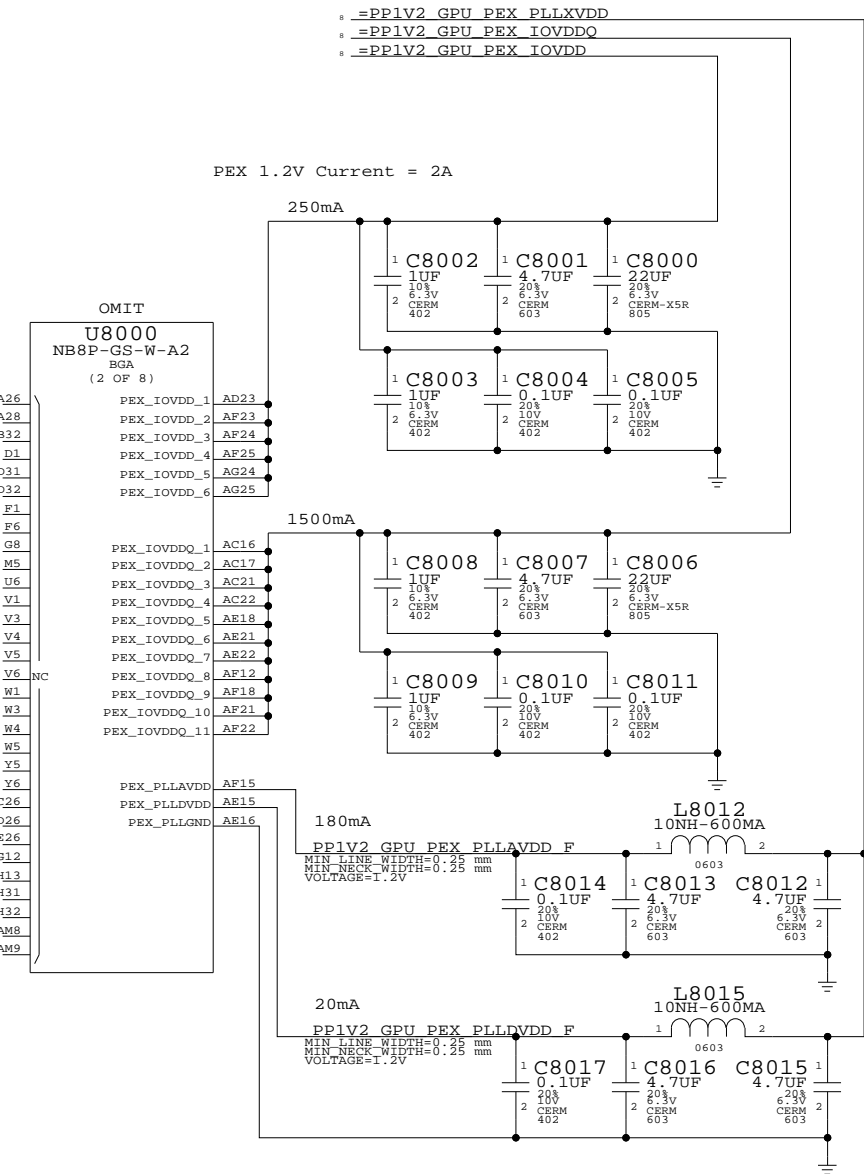
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	SCALE	NONE	SHT	65	OF	88

```
Power aliases required by this page:
- =PP1V2_GPU_PEX_PILXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)
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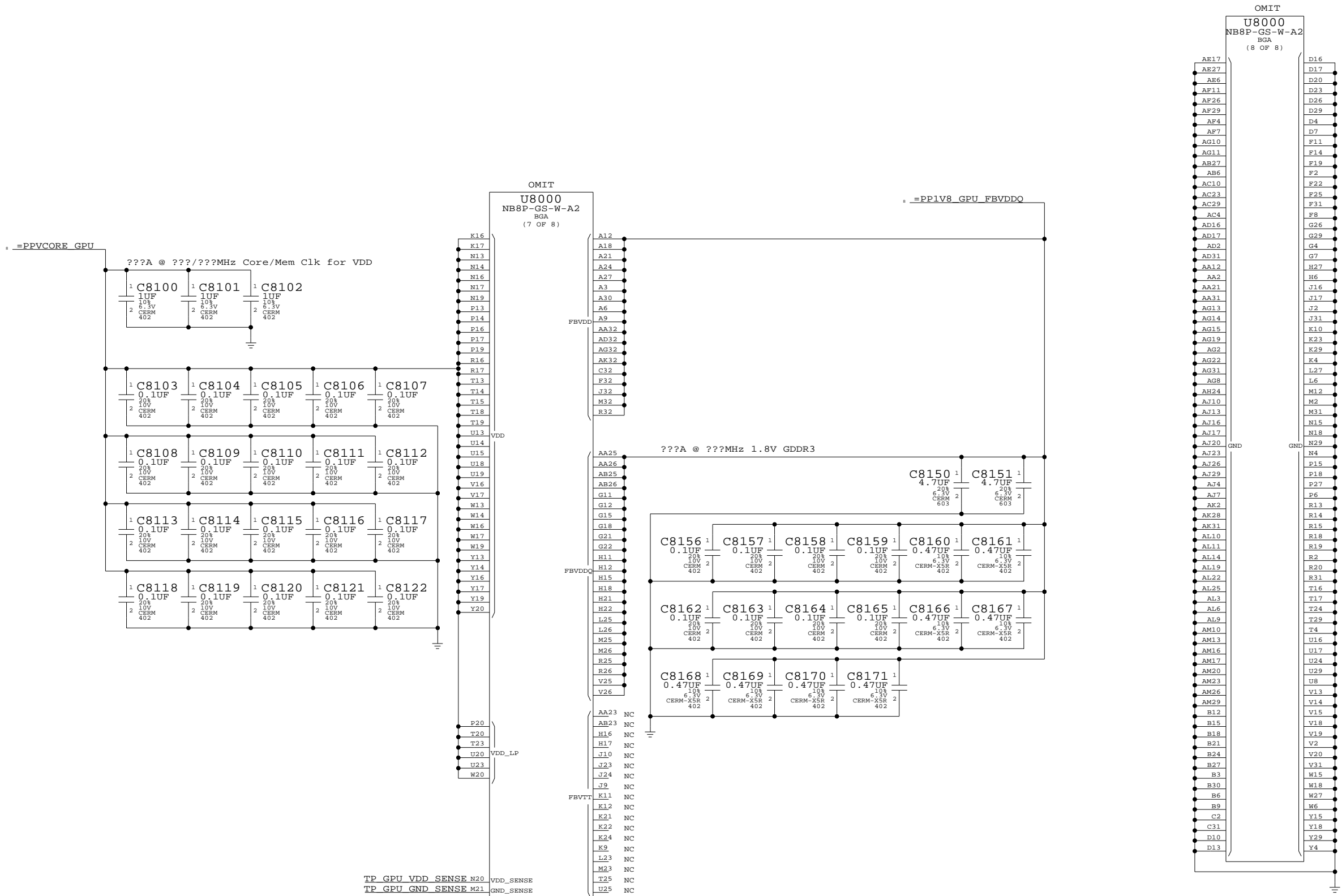
 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	A.0.0
	SCALE	SHT	OF
	NONE	66	88

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M Core/FB Power

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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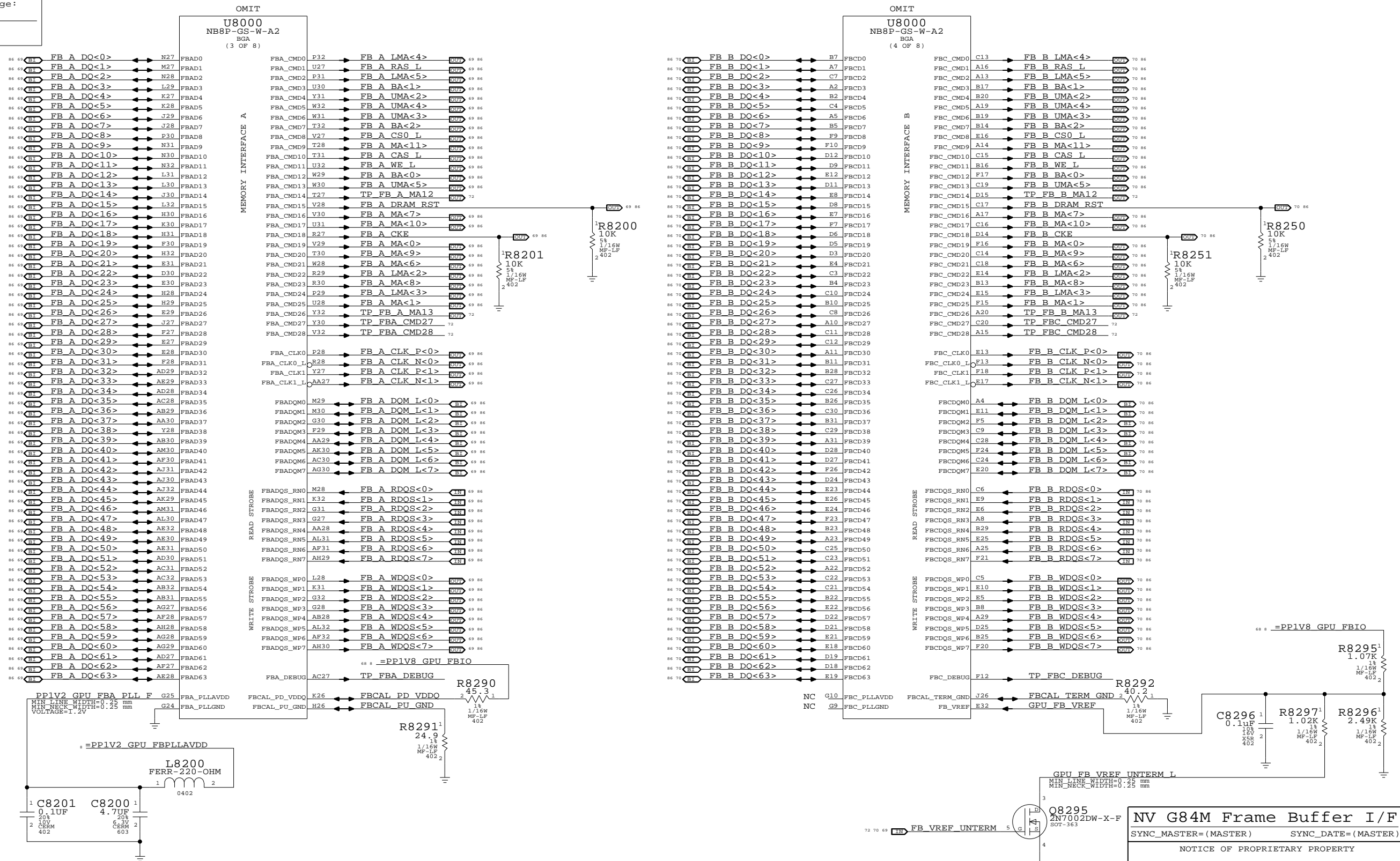
SIZE	DRAWING NUMBER	REV.
D	051-7225	A.0.0
SCALE	SHT	OF
NONE	67	88

Page Notes

Power aliases required by this page:
- =PPIV2_GPU_FBPLLAVDD
- =PPIV8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



NV G84M Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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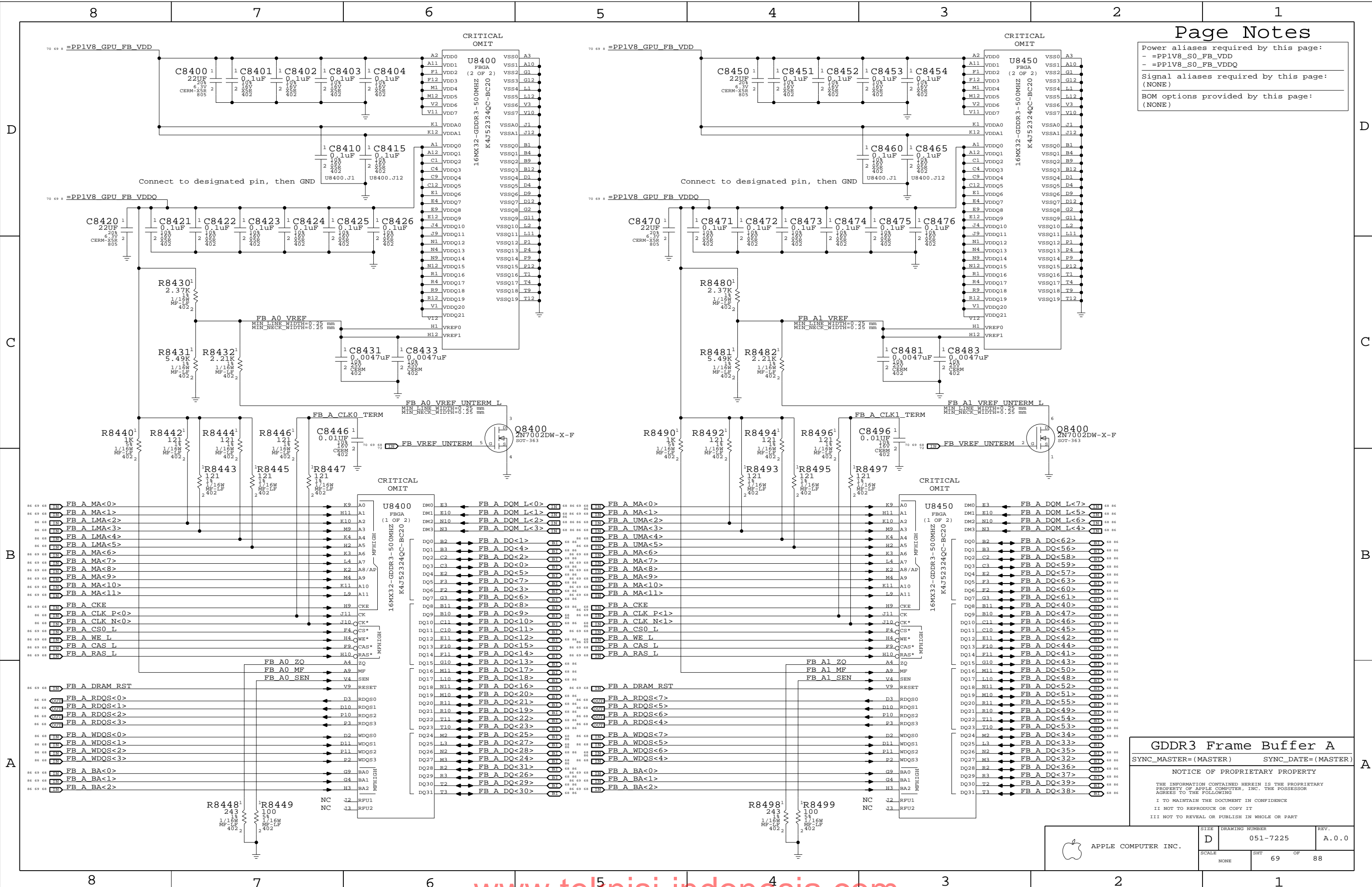
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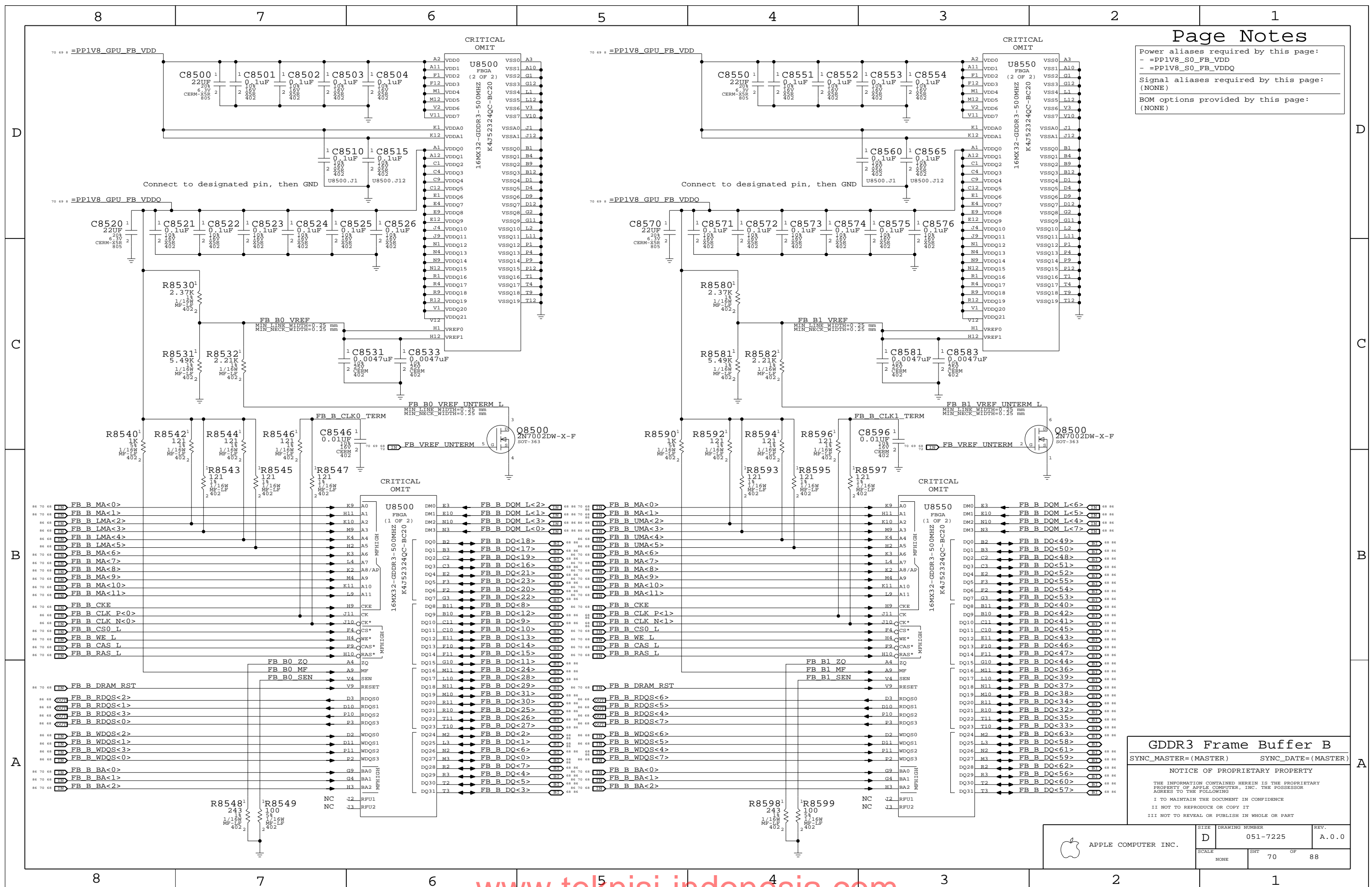
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D	051-7225	A.0.0
SCALE	SHT 68 OF 88	

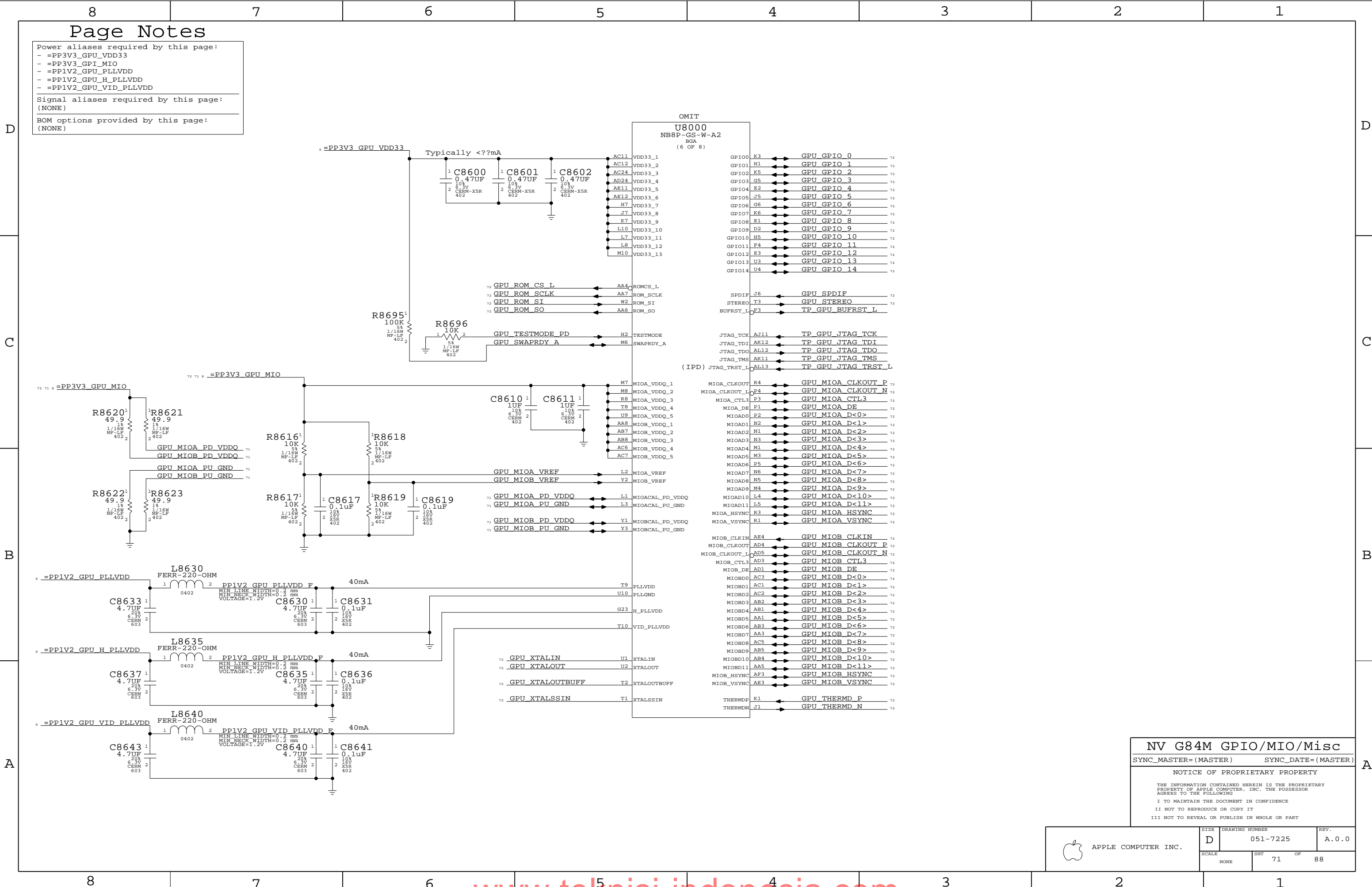
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- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)







Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPU_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT		
U8000		
NB8P-GS-W-A2		
BGA		
(6 OF 8)		
GPIO0	K3	GPU GPIO 0
GPIO1	H1	GPU GPIO 1
GPIO2	K5	GPU GPIO 2
GPIO3	G5	GPU GPIO 3
GPIO4	E2	GPU GPIO 4
GPIO5	J5	GPU GPIO 5
GPIO6	G6	GPU GPIO 6
GPIO7	K6	GPU GPIO 7
GPIO8	E1	GPU GPIO 8
GPIO9	D2	GPU GPIO 9
GPIO10	H5	GPU GPIO 10
GPIO11	F4	GPU GPIO 11
GPIO12	E3	GPU GPIO 12
GPIO13	U3	GPU GPIO 13
GPIO14	U4	GPU GPIO 14
SPDIF	J6	GPU SPDIF
STEREO	T3	GPU STEREO
BUFRST_L	F3	TP GPU BUFRST L
JTAG_TCK	AJ11	TP GPU JTAG TCK
JTAG_TDI	AK12	TP GPU JTAG TDI
JTAG_TDO	AL12	TP GPU JTAG TDO
JTAG_TMS	AK11	TP GPU JTAG TMS
(IPD) JTAG_TRST_L	AL13	TP GPU JTAG TRST L
MIOA_CLKOUT	R4	GPU MIOA CLKOUT P
MIOA_CLKOUT_L	P4	GPU MIOA CLKOUT N
MIOA_CTL3	P3	GPU MIOA CTL3
MIOA_DE	P1	GPU MIOA DE
MIOAD0	P2	GPU MIOA D<0>
MIOAD1	N2	GPU MIOA D<1>
MIOAD2	N1	GPU MIOA D<2>
MIOAD3	N3	GPU MIOA D<3>
MIOAD4	M1	GPU MIOA D<4>
MIOAD5	M3	GPU MIOA D<5>
MIOAD6	P5	GPU MIOA D<6>
MIOAD7	N6	GPU MIOA D<7>
MIOAD8	N5	GPU MIOA D<8>
MIOAD9	M4	GPU MIOA D<9>
MIOAD10	L4	GPU MIOA D<10>
MIOAD11	L5	GPU MIOA D<11>
MIOA_HSYNC	R3	GPU MIOA HSYNC
MIOA_VSYNC	R1	GPU MIOA VSYNC
MIOB_CLKIN	AE4	GPU MIOB CLKIN
MIOB_CLKOUT	AD4	GPU MIOB CLKOUT P
MIOB_CLKOUT_L	AD5	GPU MIOB CLKOUT N
MIOB_CTL3	AD3	GPU MIOB CTL3
MIOB_DE	AD1	GPU MIOB DE
MIOBD0	AC3	GPU MIOB D<0>
MIOBD1	AC1	GPU MIOB D<1>
MIOBD2	AC2	GPU MIOB D<2>
MIOBD3	AB2	GPU MIOB D<3>
MIOBD4	AB1	GPU MIOB D<4>
MIOBD5	AA1	GPU MIOB D<5>
MIOBD6	AB3	GPU MIOB D<6>
MIOBD7	AA3	GPU MIOB D<7>
MIOBD8	AC5	GPU MIOB D<8>
MIOBD9	AB5	GPU MIOB D<9>
MIOBD10	AB4	GPU MIOB D<10>
MIOBD11	AA5	GPU MIOB D<11>
MIOB_HSYNC	AF3	GPU MIOB HSYNC
MIOB_VSYNC	AE3	GPU MIOB VSYNC
THERMDP	K1	GPU THERMD P
THERMDN	J1	GPU THERMD N

NV G84M GPIO/MIO/Misc

SYNC_MASTER= (MASTER) SYNC_DATE= (MASTER)

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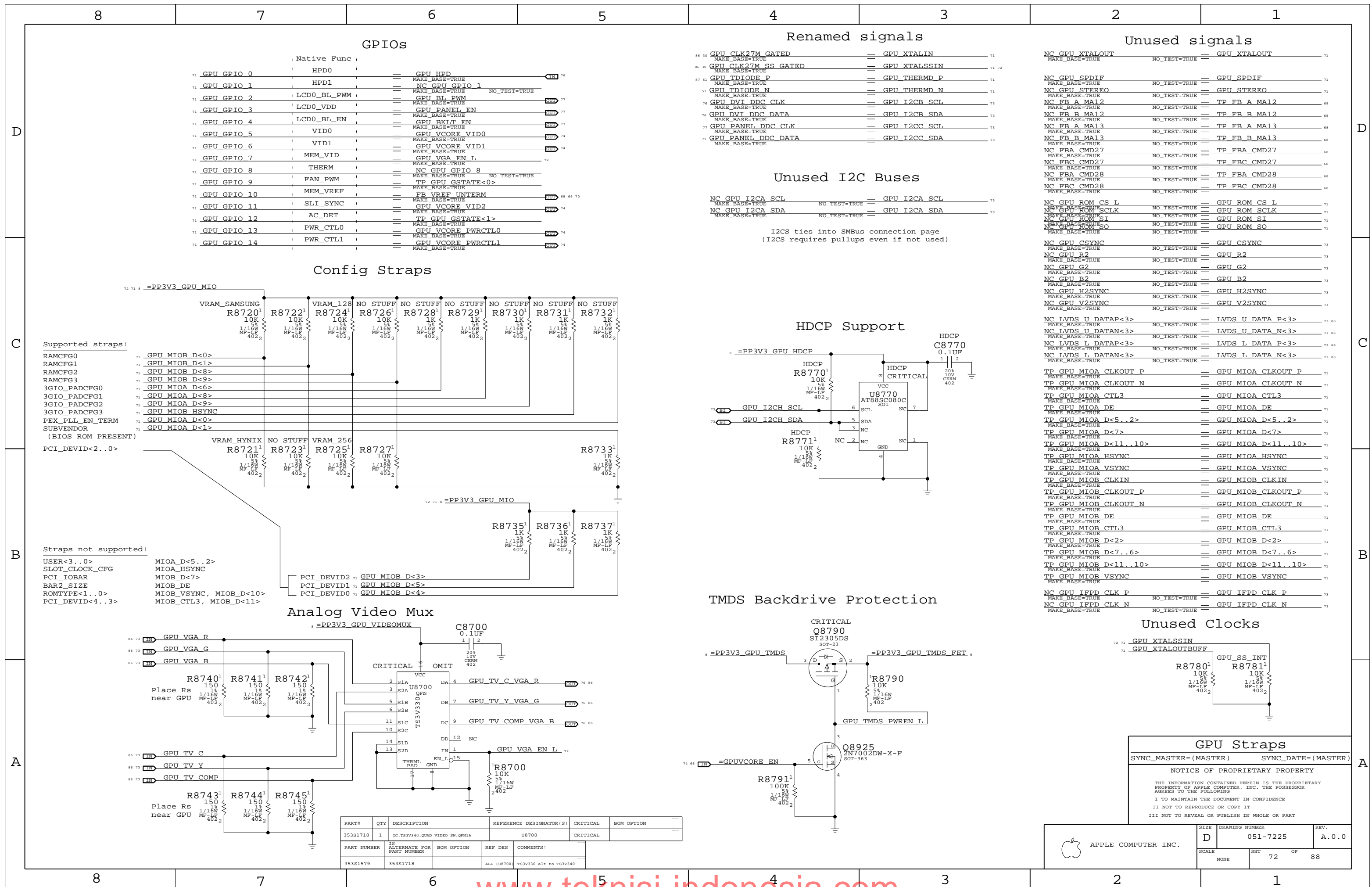
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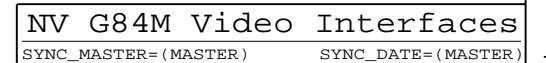
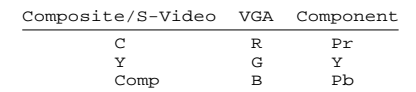
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7225	A.0.0
SCALE		SHT	71 OF 88
NONE			



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Power aliases required by this page:
- =PP1V8_GPU_IPFX
- =PP3V3_GPU_IPFCD_IOVDD
- =PP3V3_GPU_DAC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)
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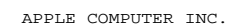
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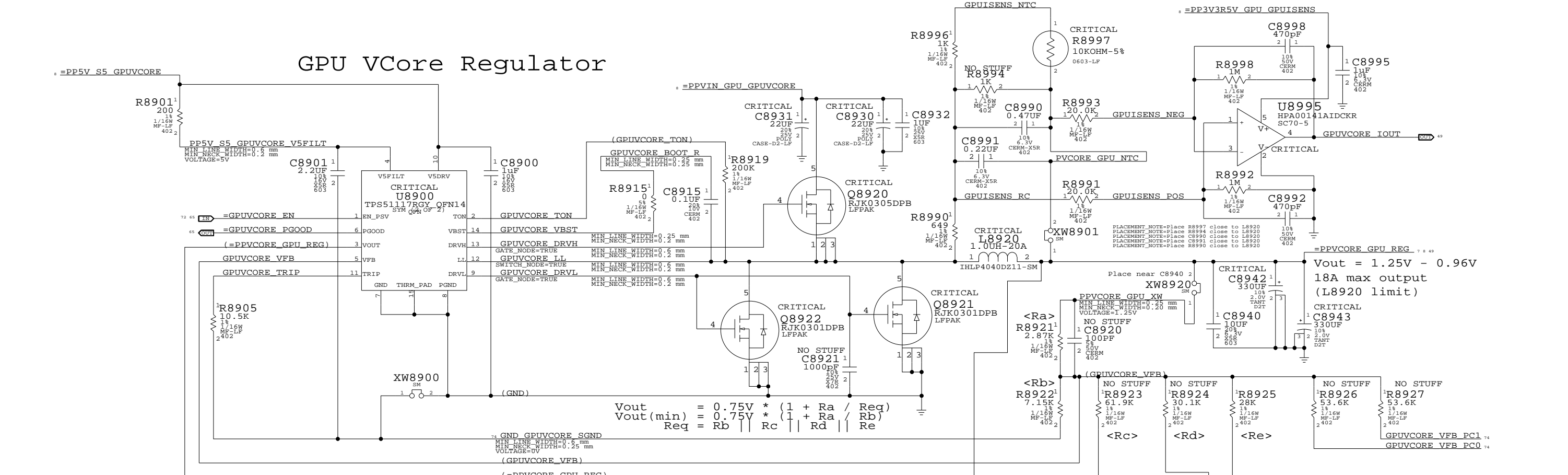
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SCALE NONE	SHT 73	OF 88

GPU VCore Regulator

GPU VCore Current Sense



GPU VCore Setpoints

VID2	VID1	VID0	C D E	State
0	0	0	- - -	1.050V (rsvd state)
0	0	1	Y - -	1.050V (max batt)
0	1	1	Y Y -	1.050V (balanced)
1	1	1	Y Y Y	1.125V (max perf)

All other states not defined

GPU (G84M) Core Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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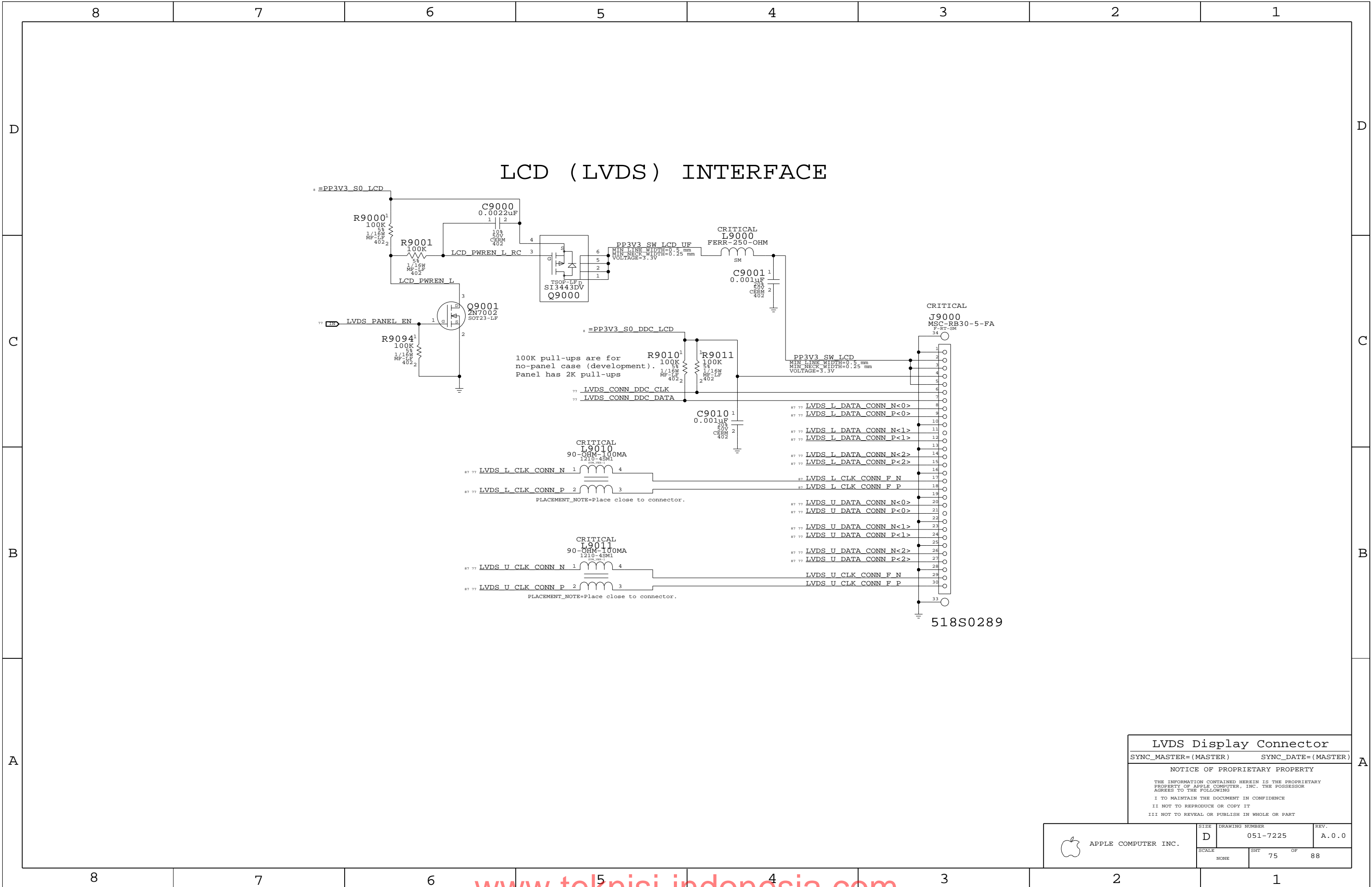
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SYNC_DATE= (MASTER)

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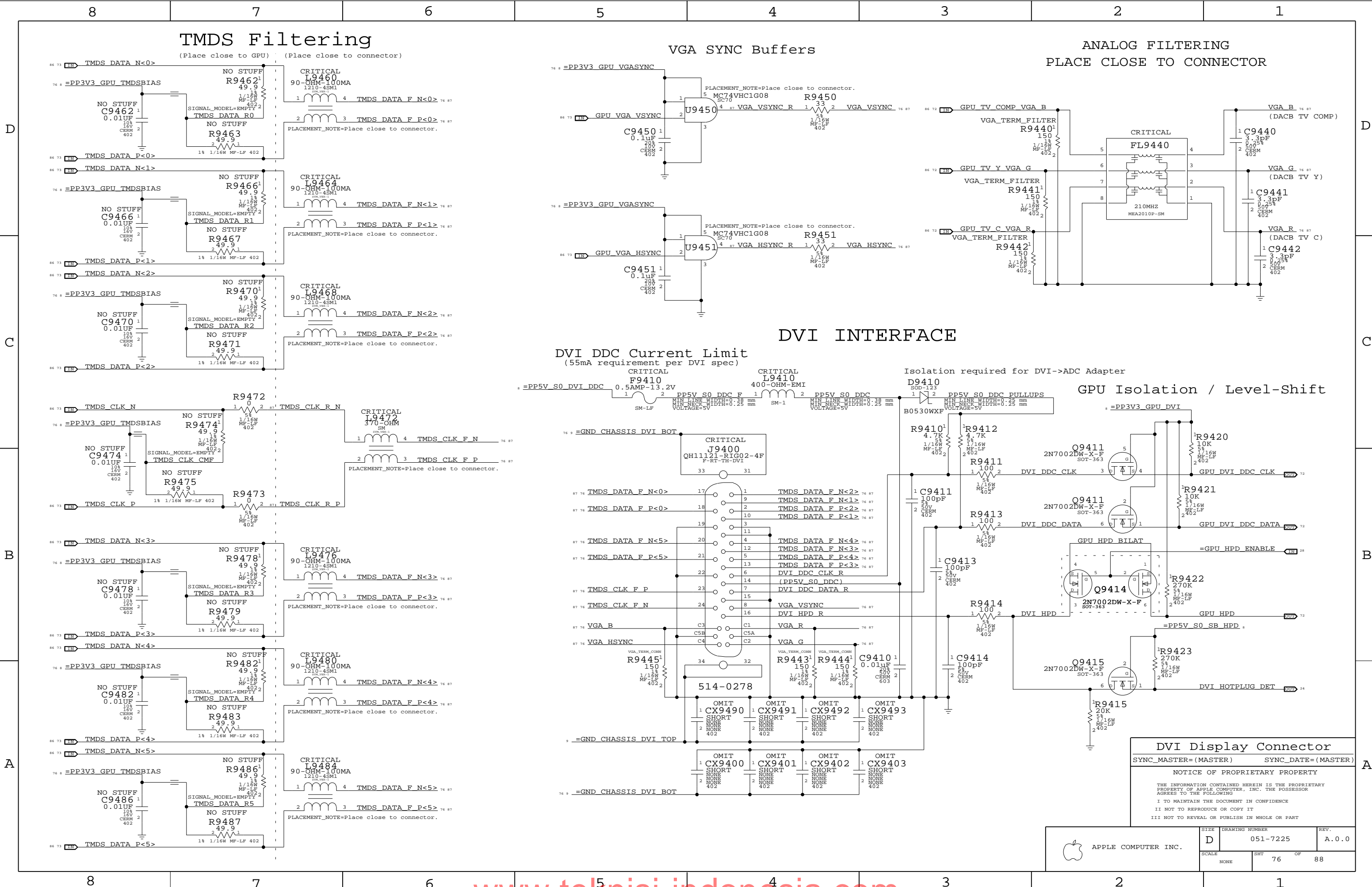
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	SCALE NONE	SHT 75	OF 88



TMDS Filtering

VGA SYNC Buffers

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

DVI INTERFACE

DVI DDC Current Limit
(55mA requirement per DVI spec)

GPU Isolation / Level-Shift

DVI Display Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE		SHT	OF
NONE		76	88

8	7	6	5	4	3	2	1
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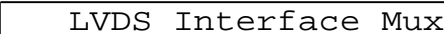
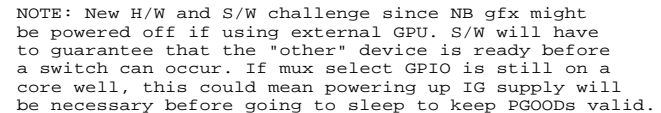


NB LVDS I/F

B



Panel/Backlight Control Mux



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DRAWING NUMBER

NUMBER

REV.

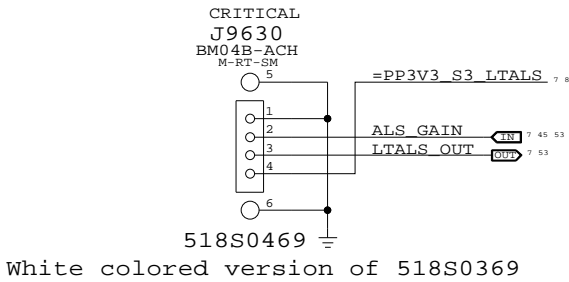
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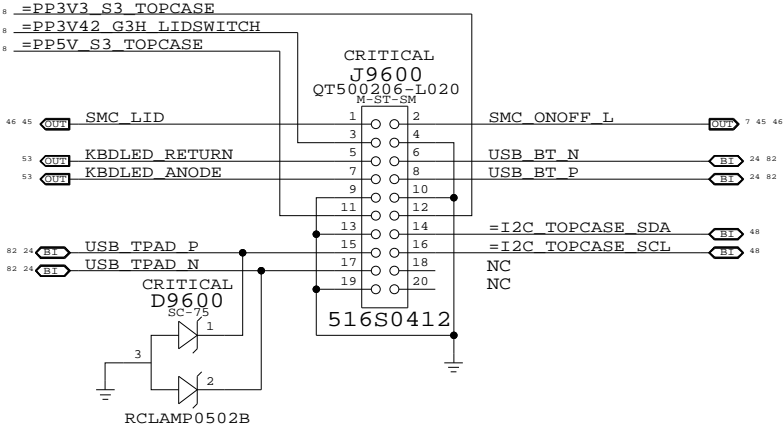
SHT

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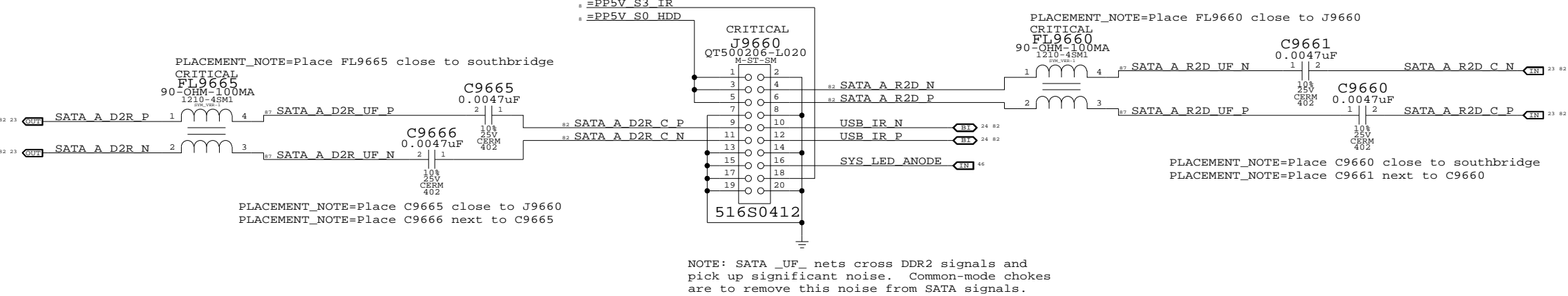
Left ALS Connector



Top-Case Connector



SATA HDD & IR & SIL Flex Connector



Project Specific Connectors

SYNC_MASTER=(M59_SYNC) SYNC_DATE=08/24/2006

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1

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer. Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.

NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB ADS L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BNR L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BPRI L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BREQ0 L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DBSY L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DEFER L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DPWR L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DRDY L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HIT L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HITM L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB LOCK L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB RS L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB TRDY L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB CPURST L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB D L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB DINV L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<0>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB D L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB DINV L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<1>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB D L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB DINV L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<2>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB D L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB DINV L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L P<3>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB DSTB L N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB A L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB REQ L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB ADSTB L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB A L<35..17>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB ADSTB L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU IERR L	10
CPU_FERR_L	CPU_55S		CPU FERR L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU PROCHOT L	10 46 58
CPU_PWRGD	CPU_55S		CPU PWRGD	7 10 13 23
CPU_FROM_SB	CPU_55S		CPU INTR	10 23
CPU_FROM_SB	CPU_55S		CPU NMI	10 23
CPU_FROM_SB	CPU_55S		CPU A20M L	10 23
CPU_FROM_SB	CPU_55S		CPU DPSLP L	7 10 23
CPU_FROM_SB	CPU_55S		CPU IGNNE L	10 23
CPU_INIT_L	CPU_55S		CPU INIT L	10 23 47
CPU_FROM_SB	CPU_55S		CPU SMI L	10 23
CPU_FROM_SB	CPU_55S		CPU STPCLK L	7 10 33
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM THRMTRIP L	10 16 23 46
FSB_CPUSLP_L	CPU_55S		FSB CPUSLP L	7 10 14
PM_DPRSLEVR	CPU_55S	CPU_2TO1	PM DPRSLPVR	7 16 25 58
(See above)	CPU_55S	CPU_2TO1	IMVP DPRSLPVR	7 58
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU BSEL<0>	10 30
(See above)	CPU_55S	CPU_2TO1	NB BSEL<0>	13 16 30
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU BSEL<1>	10 30
(See above)	CPU_55S	CPU_2TO1	NB BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU BSEL<2>	10 30
(See above)	CPU_55S	CPU_2TO1	NB BSEL<2>	13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU DPRSTP L	7 10 16 23 58
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP TCK	10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP TRST L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP BPM L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP BPM L<5>	10 13
CLK_FSB_100D	CLK_FSB	CLK_FSB	XDP CLK P	13 30 84
CLK_FSB_100D	CLK_FSB	CLK_FSB	XDP CLK N	13 30 84
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP CPURST L	13
	CPU_55S	CPU_2TO1	CPU VID<6..0>	11 12
	CPU_55S	CPU_2TO1	IMVP6 VID<6..0>	7 12 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE_P	11 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE_N	11 58
	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN_P	58
	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN_N	58

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CPU/FSB Constraints

SYNC_MASTER=T9_NAME

SYNC_DATE=01/17/2007

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PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	20 MIL	?
CRT	*	25 MIL	?
CRT_2CRT	*	20 MIL	?
CRT_SYNC	*	25 MIL	?
CRT_SYNC2SYNC	*	20 MIL	?
TVDAC	*	25 MIL	?
TVDAC_2TVDAC	*	20 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedance.
CRT & TVDAC signal single-ended impedance varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.
CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
PEG_R2D	PCIE_100D	PCIE	PEG R2D P<15..0>	56
	PCIE_100D	PCIE	PEG R2D N<15..0>	56
	PCIE_100D	PCIE	PEG R2D_C P<15..0>	15 56
	PCIE_100D	PCIE	PEG R2D_C_N<15..0>	15 56
PEG_D2R	PCIE_100D	PCIE	PEG D2R P<15..0>	15 56
	PCIE_100D	PCIE	PEG D2R N<15..0>	15 56
	PCIE_100D	PCIE	PEG D2R_C P<15..0>	56
	PCIE_100D	PCIE	PEG D2R_C_N<15..0>	56
DMI_N2S	DMI_100D	DMI	DMI N2S P<3..0>	16 24
	DMI_100D	DMI	DMI N2S N<3..0>	16 24
DMI_S2N	DMI_100D	DMI	DMI S2N P<3..0>	16 24
	DMI_100D	DMI	DMI S2N N<3..0>	16 24
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK P	15 77
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK N	15 77
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA P<2..0>	15 77
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA N<2..0>	15 77
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA P<3>	
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA N<3>	
LVDS_B_CLK	LVDS_100D	LVDS	LVDS B CLK P	15 77
LVDS_B_CLK	LVDS_100D	LVDS	LVDS B CLK N	15 77
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA P<2..0>	15 77
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA N<2..0>	15 77
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA P<3>	
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA N<3>	
LVDS_IBG		LVDS	LVDS IBG	15 22
CRT_TVO_IREF		CRT	CRT TVO IREF	
CRT_RED	CRT_50S	CRT	CRT RED	
CRT_GREEN	CRT_50S	CRT	CRT GREEN	
CRT_BLUE	CRT_50S	CRT	CRT BLUE	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT HSYNC R	
CRT_SYNC	CRT_55S	CRT_SYNC	CRT VSYNC R	
TV_A_DAC	CRT_50S	TVDAC	TV A DAC	
TV_B_DAC	CRT_50S	TVDAC	TV B DAC	
TV_C_DAC	CRT_50S	TVDAC	TV C DAC	

NB Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK P<2..0>	16 31
	MEM_70D	MEM_CLK	MEM_CLK N<2..0>	16 31
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	16 31 33
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM_CS L<1..0>	16 31 33
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A A<14..0>	16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A RAS L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A CAS L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A WE L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM A DQ<7..0>	17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM A DQ<15..8>	17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM A DQ<23..16>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM A DQ<31..24>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM A DQ<39..32>	17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM A DQ<47..40>	17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM A DQ<55..48>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM A DQ<63..56>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM A DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM A DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM A DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM A DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM A DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM A DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM A DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM A DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS P<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS N<0>	17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS P<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS N<1>	17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS P<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS N<2>	17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS P<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS N<3>	17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS P<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS N<4>	17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS P<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS N<5>	17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS P<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS N<6>	17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS P<7>	17 31
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK P<5..3>	16 32
	MEM_70D	MEM_CLK	MEM_CLK N<5..3>	16 32
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	16 32 33
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM_CS L<3..2>	16 32 33
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B A<14..0>	16 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B RAS L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B CAS L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B WE L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM B DQ<7..0>	17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM B DQ<15..8>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM B DQ<23..16>	17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM B DQ<31..24>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM B DQ<39..32>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM B DQ<47..40>	17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM B DQ<55..48>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM B DQ<63..56>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM B DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM B DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM B DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM B DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM B DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM B DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM B DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM B DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS P<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS N<0>	17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS P<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS N<1>	17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS P<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS N<2>	17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS P<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS N<3>	17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS P<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS N<4>	17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS P<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS N<5>	17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS P<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS N<6>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS P<7>	17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS N<7>	17 32

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Memory Constraints

SYNC_MASTER=T9_NOME SYNC_DATE=01/17/2007

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Disk Interface Constraints

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET			NET_TYPE	
			PHYSICAL	SPACING
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0>	
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0>	
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L	
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L	
IDE_CNTRL	IDE_55S	IDE	IDE_PDIOW_L	
IDE_PDIOIR_L	IDE_55S	IDE	IDE_PDIOIR_L	
IDE_CNTRL	IDE_55S	IDE	IDE_PDDACK_L	
IDE_CNTRL	IDE_55S	IDE	IDE_PDDREQ	
IDE_PDIOIRDY	IDE_55S	IDE	IDE_PDIOIRDY	
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14	
IDE_RST_I	IDE_55S	IDE	ODD_RST_5VTOL_L	
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_P	
	SATA_100D	SATA	SATA_A_R2D_C_N	
	SATA_100D	SATA	SATA_A_R2D_P	
	SATA_100D	SATA	SATA_A_R2D_N	
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R_P	
	SATA_100D	SATA	SATA_A_D2R_N	
	SATA_100D	SATA	SATA_A_D2R_C_P	
	SATA_100D	SATA	SATA_A_D2R_C_N	
SATA_B_R2D	SATA_100D	SATA	SATA_B_R2D_C_P	
	SATA_100D	SATA	SATA_B_R2D_C_N	
	SATA_100D	SATA	SATA_B_R2D_P	
	SATA_100D	SATA	SATA_B_R2D_N	
SATA_B_D2R	SATA_100D	SATA	SATA_B_D2R_P	
	SATA_100D	SATA	SATA_B_D2R_N	
	SATA_100D	SATA	SATA_B_D2R_C_P	
	SATA_100D	SATA	SATA_B_D2R_C_N	
SATA_C_R2D	SATA_100D	SATA	SATA_C_R2D_C_P	
	SATA_100D	SATA	SATA_C_R2D_C_N	
	SATA_100D	SATA	SATA_C_R2D_P	
	SATA_100D	SATA	SATA_C_R2D_N	
SATA_C_D2R	SATA_100D	SATA	SATA_C_D2R_P	
	SATA_100D	SATA	SATA_C_D2R_N	
	SATA_100D	SATA	SATA_C_D2R_C_P	
	SATA_100D	SATA	SATA_C_D2R_C_N	
SATA_RBIA5	SATA_55S		SATA_RBIA5	
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	
	HDA_55S	HDA	HDA_BIT_CLK_R	
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	
	HDA_55S	HDA	HDA_SYNC_R	
HDA_RST_I	HDA_55S	HDA	HDA_RST_L	
	HDA_55S	HDA	HDA_RST_L_R	
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOIT	HDA_55S	HDA	HDA_SDOIT	
	HDA_55S	HDA	HDA_SDOIT_R	
USB_EXT_A	USB_90D	USB	USB_EXT_A_P	
	USB_90D	USB	USB_EXT_A_N	
	USB_90D	USB	USB_EXT_A_MUXED_P	
	USB_90D	USB	USB_EXT_A_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	
	USB_90D	USB	USB_MINI_N	
USB_EXTD	USB_90D	USB	USB_EXTD_P	
	USB_90D	USB	USB_EXTD_N	
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	
	USB_90D	USB	USB_CAMERA_N	
USB_BT	USB_90D	USB	USB_BT_P	
	USB_90D	USB	USB_BT_N	
USB_TPAD	USB_90D	USB	USB_TPAD_P	
	USB_90D	USB	USB_TPAD_N	
USB_IR	USB_90D	USB	USB_IR_P	
	USB_90D	USB	USB_IR_N	
USB_EXTRB	USB_90D	USB	USB_EXTRB_P	
	USB_90D	USB	USB_EXTRB_N	
USB_EXCARD	USB_90D	USB	USB_EXCARD_P	
	USB_90D	USB	USB_EXCARD_N	
USB_EXTC	USB_90D	USB	USB_EXTC_P	
	USB_90D	USB	USB_EXTC_N	
USB_RBIA5	USB_60S		USB_RBIA5	
SMB_SB_SCL	SMB_55S	SMB	SMB_CLK	
SMB_SB_SDA	SMB_55S	SMB	SMB_DATA	
SMB_SB_ME_SCL	SMB_55S	SMB	SMB_ME_CLK	
SMB_SB_ME_SDA	SMB_55S	SMB	SMB_ME_DATA	
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R	
	SPI_55S	SPI	SPI_SCLK	
	SPI_55S	SPI	SPI_A_SCLK_R	
	SPI_55S	SPI	SPI_B_SCLK_R	
SPI_SI	SPI_55S	SPI	SPI_SI_R	
	SPI_55S	SPI	SPI_SI	
	SPI_55S	SPI	SPI_A_SI_R	
	SPI_55S	SPI	SPI_B_SI_R	
SPI_SO	SPI_55S	SPI	SPI_SO	
	SPI_55S	SPI	SPI_A_SO_R	
	SPI_55S	SPI	SPI_B_SO	
	SPI_55S	SPI	SPI_B_SO_R	
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R_L<0>	
	SPI_55S	SPI	SPI_CE_L<0>	
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R_L<1>	
	SPI_55S	SPI	SPI_CE_L<1>	


SB Constraints (1 of 2)

SYNC_MASTER=T9_NOME	SYNC_DATE=01/17/2007
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	SCALE	SHT	OF
	NONE	82	88

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MILS	?

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET

NET_TYPE

PHYSICAL

SPACING

PCI_AD<18..0>

PCI_AD<19>

PCI_AD<20>

PCI_AD<31..21>

PCI_PAR

PCI_C_BE_L<3..0>

PCI_IRDY_L

PCI_DEVSEL_L

PCI_PERR_L

PCI_LOCK_L

PCI_SERR_L

PCI_STOP_L

PCI_TRDY_L

PCI_FRAME_L

PCI_FW_REQ_L

PCI_FW_GNT_L

PCI_REQ1_L

PCI_GNT1_L

PCI_REQ2_L

PCI_GNT2_L

INT_PIRQA_L

INT_PIRQB_L

INT_PIROC_L

INT_PIROD_L

INT_PIROE_L

INT_PIROF_L

PCIE_A_R2D_C_P

PCIE_A_R2D_C_N

PCIE_A_D2R_P

PCIE_A_D2R_N

PCIE_B_R2D_C_P

PCIE_B_R2D_C_N

PCIE_B_D2R_P

PCIE_B_D2R_N

PCIE_EXCARD_R2D_C_P

PCIE_EXCARD_R2D_C_N

PCIE_EXCARD_D2R_P

PCIE_EXCARD_D2R_N

PCIE_FW_R2D_C_P

PCIE_FW_R2D_C_N

PCIE_FW_D2R_P

PCIE_FW_D2R_N

PCIE_MINI_R2D_C_P

PCIE_MINI_R2D_C_N

PCIE_MINI_D2R_P

PCIE_MINI_D2R_N

GLAN_COMP

CLINK_NB_CLK

CLINK_NB_DATA

CLINK_NB_RESET_L

CLINK_WLAN_CLK

CLINK_WLAN_DATA

CLINK_WLAN_RESET_L

NB_CLINK_VREF

SB_CLINK_VREF0

SB_CLINK_VREF1

PCIE_ENET_R2D_C_P

PCIE_ENET_R2D_C_N

PCIE_ENET_R2D_P

PCIE_ENET_R2D_N

PCIE_ENET_D2R_P

PCIE_ENET_D2R_N

PCIE_ENET_D2R_C_P

PCIE_ENET_D2R_C_N

ENET_MDI_P<0>

ENET_MDI_N<0>

ENET_MDI_P<1>

ENET_MDI_N<1>

ENET_MDI_P<2>

ENET_MDI_N<2>

ENET_MDI_P<3>

ENET_MDI_N<3>

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SB Constraints (2 of 2)

SYNC_MASTER=T9_NAME

SYNC_DATE=01/17/2007

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DRAWING NUMBER 051-7225

REV. A.0.0

SCALE NONE

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4

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Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	CK505_CPUH	CLK_FSB_100D	CLK_FSB	CK505_CPU0_P
	CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_N
	CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_P
	CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_N
	CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_P
	CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_N
	CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0_CLK_ITPEN
	CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1_CLK
	CK505_PCI1	CLK_MED_55S	CLK_MED	CK505_PCI1_CLK
	CK505_PCI2	CLK_MED_55S	CLK_MED	CK505_PCI2_CLK
	CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3_CLK
	CK505_PCI4	CLK_MED_55S	CLK_MED	CK505_PCI4_CLK
	CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5_CLK_FCTSEL
	(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA
	(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC
	CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_P
	CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_N
	CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_P
	CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_N
	CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P
	CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N
	CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_P
	CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_N
	CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P
	CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N
	CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P
	CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N
	CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_P
	CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_N
	CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_P
	CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_N
	CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P
	CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N
	CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P
	CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N
	(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P
	(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N
	(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P
	(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N
	(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P
	(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N
	(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS
	(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB
	(CK505_PCI1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW
	(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM
	(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC
	(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR
	(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER
	(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA
	(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC
	(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_P
	(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_N
	(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P
	(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N
	CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P
	CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N
	CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P
	CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N
	CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P
	CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N
	CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P
	CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N
	CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P
	CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N
	CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P
	CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N
	(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7 is project-specific
	(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P
	(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL
	SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA
	SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL
	SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA
	SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL
	SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA
	SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL
	SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA
	SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL
	SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA

Clock & SMC Constraints

SYNC_MASTER=T9_NOME

SYNC_DATE=01/17/2007

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE		
	PHYSICAL	SPACING	
<input type="checkbox"/> FW_D_CTL	FW_55S	FW	FW LINK<7..0>
<input type="checkbox"/> FW_D_CTL	FW_55S	FW	FW CTL<1..0>
<input type="checkbox"/> FW_L_CLK	CLK_MED_55S	CLK_MED	CLKFW LINK_LCLK
<input type="checkbox"/> FW_L_CLK	CLK_MED_55S	CLK_MED	CLKFW PHY_LCLK 38 39
<input type="checkbox"/> FW_P_CLK	CLK_MED_55S	CLK_MED	CLKFW LINK_PCLK 38 39
<input type="checkbox"/> FW_P_CLK	CLK_MED_55S	CLK_MED	CLKFW PHY_PCLK
<input type="checkbox"/> FW_LKON	FW_55S	FW	FW LKON
<input type="checkbox"/> FW_LKON	FW_55S	FW	FW LKON_R
<input type="checkbox"/> FW_LPS	FW_55S	FW	FW LPS 38 39
<input type="checkbox"/> FW_LREQ	FW_55S	FW	FW LREQ 38 39
<input type="checkbox"/> FW_PINT	FW_55S	FW	FW PINT 38 39
<input type="checkbox"/> FWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI_R
<input type="checkbox"/> FWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI
<input type="checkbox"/> FW_0_TPA	FW_110D	FW_TP	FW_0_TPA_P 39 41
<input type="checkbox"/> FW_0_TPA	FW_110D	FW_TP	FW_0_TPA_N 39 41
<input type="checkbox"/> FW_0_TPB	FW_110D	FW_TP	FW_0_TPB_P 39 41
<input type="checkbox"/> FW_0_TPB	FW_110D	FW_TP	FW_0_TPB_N 39 41
<input type="checkbox"/> FW_1_TPA	FW_110D	FW_TP	FW_1_TPA_P 39 41
<input type="checkbox"/> FW_1_TPA	FW_110D	FW_TP	FW_1_TPA_N 39 41
<input type="checkbox"/> FW_1_TPB	FW_110D	FW_TP	FW_1_TPB_P 39 41
<input type="checkbox"/> FW_1_TPB	FW_110D	FW_TP	FW_1_TPB_N 39 41
Port 2 Not Used			

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FireWire Constraints

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APPLE COMPUTER INC.

SIZE	D	DRAWING NUMBER	051-7225	REV.	A.0.0
SCALE	NONE	SHT	85	OF	88

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8			7			6	
GDDR3 Frame Buffer Signal Constraints							
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFAIR PRIMARY GAP	DIFFAIR NECK GAP
GDDR3_40R50SE	*	=50_OHM_SE	=40_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR3_50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TMD5_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
VGA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TMDS	*	20 MIL	?
VGA	*	20 MIL	?
VGA_SYNC	*	20 MIL	?

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
<div></div>	FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB A CLK P<0>	68 69
<div></div>		GDDR3_80D	GDDR3_CLK	FB A CLK N<0>	68 69
<div></div>	FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB A CLK P<1>	68 69
<div></div>		GDDR3_80D	GDDR3_CLK	FB A CLK N<1>	68 69
<div></div>	FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A MA<1..0>	68 69
<div></div>	FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A MA<11..6>	68 69
<div></div>	FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A BA<2..0>	68 69
<div></div>	FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A RAS L	68 69
<div></div>	FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A CAS L	68 69
<div></div>	FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A WE L	68 69
<div></div>	FB_AB_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB A CEK	68 69
<div></div>	FB_AB_CMD	GDDR3_40R50SE	GDDR3_CMD	FB A CS0 L	68 69
<div></div>	FB_AB_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB A DRAM_RST	68 69
<div></div>	FB_A_CMD	GDDR3_50SE	GDDR3_CMD	FB A LMA<5..2>	68 69
<div></div>	FB_B_CMD	GDDR3_50SE	GDDR3_CMD	FB A UMA<5..2>	68 69
<div></div>	FB_A_WDQS0	GDDR3_50SE	GDDR3_DQS	FB A WDQS<0>	68 69
<div></div>	FB_A_WDQS1	GDDR3_50SE	GDDR3_DQS	FB A WDQS<1>	68 69
<div></div>	FB_A_WDQS2	GDDR3_50SE	GDDR3_DQS	FB A WDQS<2>	68 69
<div></div>	FB_A_WDQS3	GDDR3_50SE	GDDR3_DQS	FB A WDQS<3>	68 69
<div></div>	FB_A_RDQS0	GDDR3_50SE	GDDR3_DQS	FB A RDQS<0>	68 69
<div></div>	FB_A_RDQS1	GDDR3_50SE	GDDR3_DQS	FB A RDQS<1>	68 69
<div></div>	FB_A_RDQS2	GDDR3_50SE	GDDR3_DQS	FB A RDQS<2>	68 69
<div></div>	FB_A_RDQS3	GDDR3_50SE	GDDR3_DQS	FB A RDQS<3>	68 69
<div></div>	FB_A_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB A DQ<7..0>	68 69
<div></div>	FB_A_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB A DQ<15..8>	68 69
<div></div>	FB_A_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB A DQ<23..16>	68 69
<div></div>	FB_A_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB A DQ<31..24>	68 69
<div></div>	FB_A_DQM0	GDDR3_50SE	GDDR3_DATA	FB A DQM L<0>	68 69
<div></div>	FB_A_DQM1	GDDR3_50SE	GDDR3_DATA	FB A DQM L<1>	68 69
<div></div>	FB_A_DQM2	GDDR3_50SE	GDDR3_DATA	FB A DQM L<2>	68 69
<div></div>	FB_A_DQM3	GDDR3_50SE	GDDR3_DATA	FB A DQM L<3>	68 69
<div></div>	FB_B_WDQS0	GDDR3_50SE	GDDR3_DQS	FB A WDQS<4>	68 69
<div></div>	FB_B_WDQS1	GDDR3_50SE	GDDR3_DQS	FB A WDQS<5>	68 69
<div></div>	FB_B_WDQS2	GDDR3_50SE	GDDR3_DQS	FB A WDQS<6>	68 69
<div></div>	FB_B_WDQS3	GDDR3_50SE	GDDR3_DQS	FB A WDQS<7>	68 69
<div></div>	FB_B_RDQS0	GDDR3_50SE	GDDR3_DQS	FB A RDQS<4>	68 69
<div></div>	FB_B_RDQS1	GDDR3_50SE	GDDR3_DQS	FB A RDQS<5>	68 69
<div></div>	FB_B_RDQS2	GDDR3_50SE	GDDR3_DQS	FB A RDQS<6>	68 69
<div></div>	FB_B_RDQS3	GDDR3_50SE	GDDR3_DQS	FB A RDQS<7>	68 69
<div></div>	FB_B_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB A DQ<39..32>	68 69
<div></div>	FB_B_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB A DQ<47..40>	68 69
<div></div>	FB_B_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB A DQ<55..48>	68 69
<div></div>	FB_B_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB A DQ<63..56>	68 69
<div></div>	FB_B_DQM0	GDDR3_50SE	GDDR3_DATA	FB A DQM L<4>	68 69
<div></div>	FB_B_DQM1	GDDR3_50SE	GDDR3_DATA	FB A DQM L<5>	68 69
<div></div>	FB_B_DQM2	GDDR3_50SE	GDDR3_DATA	FB A DQM L<6>	68 69
<div></div>	FB_B_DQM3	GDDR3_50SE	GDDR3_DATA	FB A DQM L<7>	68 69

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
		PHYSICAL	SPACING		
	FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB B CLK P<0>	68 70
		GDDR3_80D	GDDR3_CLK	FB B CLK N<0>	68 70
	FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB B CLK P<1>	68 70
		GDDR3_80D	GDDR3_CLK	FB B CLK N<1>	68 70
	FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B MA<1..0>	68 70
	FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B MA<11..6>	68 70
	FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B BA<2..0>	68 70
	FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B RAS_L	68 70
	FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B CAS_L	68 70
	FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B WE_L	68 70
	FB_CD_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB B CEK	68 70
	FB_CD_CMD	GDDR3_40R50SE	GDDR3_CMD	FB B CS0_L	68 70
	FB_CD_CMD_PD	GDDR3_40R50SE	GDDR3_CMD	FB B DRAM_RST	68 70
	FB_C_CMD	GDDR3_50SE	GDDR3_CMD	FB B LMA<5..2>	68 70
	FB_D_CMD	GDDR3_50SE	GDDR3_CMD	FB B UMA<5..2>	68 70
	FB_C_WDQS0	GDDR3_50SE	GDDR3_PQS	FB B WDQS<0>	68 70
	FB_C_WDQS1	GDDR3_50SE	GDDR3_PQS	FB B WDQS<1>	68 70
	FB_C_WDQS2	GDDR3_50SE	GDDR3_PQS	FB B WDQS<2>	68 70
	FB_C_WDQS3	GDDR3_50SE	GDDR3_PQS	FB B WDQS<3>	68 70
	FB_C_RDQS0	GDDR3_50SE	GDDR3_PQS	FB B RDQS<0>	68 70
	FB_C_RDQS1	GDDR3_50SE	GDDR3_PQS	FB B RDQS<1>	68 70
	FB_C_RDQS2	GDDR3_50SE	GDDR3_PQS	FB B RDQS<2>	68 70
	FB_C_RDQS3	GDDR3_50SE	GDDR3_PQS	FB B RDQS<3>	68 70
	FB_C_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB B DQ<7..0>	68 70
	FB_C_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB B DQ<15..8>	68 70
	FB_C_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB B DQ<23..16>	68 70
	FB_C_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB B DQ<31..24>	68 70
	FB_C_DQM0	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<0>	68 70
	FB_C_DQM1	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<1>	68 70
	FB_C_DQM2	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<2>	68 70
	FB_C_DQM3	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<3>	68 70
	FB_D_WDQS0	GDDR3_50SE	GDDR3_PQS	FB B WDQS<4>	68 70
	FB_D_WDQS1	GDDR3_50SE	GDDR3_PQS	FB B WDQS<5>	68 70
	FB_D_WDQS2	GDDR3_50SE	GDDR3_PQS	FB B WDQS<6>	68 70
	FB_D_WDQS3	GDDR3_50SE	GDDR3_PQS	FB B WDQS<7>	68 70
	FB_D_RDQS0	GDDR3_50SE	GDDR3_PQS	FB B RDQS<4>	68 70
	FB_D_RDQS1	GDDR3_50SE	GDDR3_PQS	FB B RDQS<5>	68 70
	FB_D_RDQS2	GDDR3_50SE	GDDR3_PQS	FB B RDQS<6>	68 70
	FB_D_RDQS3	GDDR3_50SE	GDDR3_PQS	FB B RDQS<7>	68 70
	FB_D_DQ_BYTE0	GDDR3_50SE	GDDR3_DATA	FB B DQ<39..32>	68 70
	FB_D_DQ_BYTE1	GDDR3_50SE	GDDR3_DATA	FB B DQ<47..40>	68 70
	FB_D_DQ_BYTE2	GDDR3_50SE	GDDR3_DATA	FB B DQ<55..48>	68 70
	FB_D_DQ_BYTE3	GDDR3_50SE	GDDR3_DATA	FB B DQ<63..56>	68 70
	FB_D_DQM0	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<4>	68 70
	FB_D_DQM1	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<5>	68 70
	FB_D_DQM2	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<6>	68 70
	FB_D_DQM3	GDDR3_50SE	GDDR3_DATA	FB B DQM_L<7>	68 70

G84M Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
(CK505_DOT96)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M 30
	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_GATED 30 72
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS 30
	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS_GATED 30
	LVDS_100D	LVDS	LVDS_L_CLK_P 73 77
	LVDS_100D	LVDS	LVDS_L_CLK_N 73 77
	LVDS_100D	LVDS	LVDS_L_DATA_P<3..0> 7 72
	LVDS_100D	LVDS	LVDS_L_DATA_N<3..0> 7 72
	LVDS_100D	LVDS	LVDS_U_CLK_P 73 77
	LVDS_100D	LVDS	LVDS_U_CLK_N 73 77
	LVDS_100D	LVDS	LVDS_U_DATA_P<3..0> 72 73
	LVDS_100D	LVDS	LVDS_U_DATA_N<3..0> 72 73
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_P 73 76
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_N 73 76
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_P<5..0> 73 76
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_N<5..0> 73 76
VGA_R_TV_C	VGA_50S	VGA	GPU_TV_C_VGA_R 72 76
VGA_G_TV_Y	VGA_50S	VGA	GPU_TV_Y_VGA_G 72 76
VGA_B_TV_COMP	VGA_50S	VGA	GPU_TV_COMP_VGA_B 72 76
	VGA_50S	VGA	GPU_VGA_R 72 73
	VGA_50S	VGA	GPU_VGA_G 72 73
	VGA_50S	VGA	GPU_VGA_B 72 73
	VGA_50S	VGA	GPU_TV_C 72 73
	VGA_50S	VGA	GPU_TV_Y 72 73
	VGA_50S	VGA	GPU_TV_COMP 72 73
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_HSYNC 73 76
VGA_SYNC	VGA_55S	VGA_SYNC	GPU_VGA_VSYNC 73 76

GPU (G84M) Constraints

SYNC_MASTER= (MASTER)	SYNC_DATE= (MASTER)
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SCALE

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8		7		6		5		4		3		2		1				
M75 Board-Specific Spacing & Physical Constraints																		
BOARD LAYERS								BOARD AREAS				BOARD UNITS (MIL or MM)		ALLEGRO VERSION				
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM								NO_TYPE, BGA				MM		15.5.1				
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT	NET_SPACING_TYPE1		NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DEFAULT		*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM	DEFAULT		*	0.1 MM	?	*		*	BGA	BGA_P1MM
STANDARD		*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT	STANDARD		*	=DEFAULT	?	MEM_CLK		*	BGA	BGA_P2MM
									BGA_P1MM		*	=DEFAULT	?	CLK_FSB		*	BGA	BGA_P2MM
									BGA_P2MM		*	=DEFAULT	?	CLK_PCIE		*	BGA	BGA_P2MM
									BGA_P3MM		*	=DEFAULT	?	CLK_MED		*	BGA	BGA_P2MM
														CLK_SLOW		*	BGA	BGA_P2MM
														FSB_DSTB		FSB_DSTB	BGA	BGA_P3MM
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	SPACING_RULE_SET		LAYER	LINE-TO-LINE SPACING	WEIGHT					
55_OHM_SE		TOP, BOTTOM	Y	0.100 MM	0.100 MM				1.5:1_SPACING		*	0.15 MM	?					
55_OHM_SE		ISL2, ISL11	Y	0.250 MM	0.076 MM				1.8:1_SPACING		*	0.18 MM	?					
55_OHM_SE		*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD	2:1_SPACING		*	0.2 MM	?					
									2.5:1_SPACING		*	0.25 MM	?					
									3:1_SPACING		*	0.3 MM	?					
									4:1_SPACING		*	0.4 MM	?					
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP										
50_OHM_SE		TOP, BOTTOM	Y	0.125 MM	0.125 MM													
50_OHM_SE		*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD										
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP										
45_OHM_SE		TOP, BOTTOM	Y	0.150 MM	0.150 MM													
45_OHM_SE		*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD										
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP										
40_OHM_SE		TOP, BOTTOM	Y	0.185 MM	0.185 MM													
40_OHM_SE		*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD										
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP										
27P4_OHM_SE		TOP, BOTTOM	Y	0.335 MM	0.335 MM													
27P4_OHM_SE		*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD										
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
70_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	1:1_DIFFPAIR		*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM	
70_OHM_DIFF		ISL3, ISL4	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM										
70_OHM_DIFF		ISL9, ISL10	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM										
70_OHM_DIFF		ISL2, ISL11	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM										
70_OHM_DIFF		TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM										
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP										
80_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD										
80_OHM_DIFF		ISL3, ISL4	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM										
80_OHM_DIFF		ISL9, ISL10	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM										
80_OHM_DIFF		ISL2, ISL11	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM										
80_OHM_DIFF		TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM										
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP										
85_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD										
85_OHM_DIFF		ISL3, ISL4	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM										
85_OHM_DIFF		ISL9, ISL10	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM										
85_OHM_DIFF		ISL2, ISL11	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM										
85_OHM_DIFF		TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM										
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP										
90_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD										
90_OHM_DIFF		ISL3, ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM										
90_OHM_DIFF		ISL9, ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM										
90_OHM_DIFF		ISL2, ISL11	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM										
90_OHM_DIFF		TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM										
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP										
100_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD										
100_OHM_DIFF		ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM										
100_OHM_DIFF		ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM										
100_OHM_DIFF		ISL2, ISL11	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM										
100_OHM_DIFF		TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM										
PHYSICAL_RULE_SET		LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP										
110_OHM_DIFF		*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD										
110_OHM_DIFF		ISL3, ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM										
110_OHM_DIFF		ISL9, ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM										
110_OHM_DIFF		ISL2, ISL11	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM										
110_OHM_DIFF		TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM										
NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.																		
PCB Rule Definitions																		
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)																		
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